

# HuaQin Confidential

## IRON FIST\_XM AIR 13.3 EU \_M/B Schematics Document

Intel Kabylake Y-Processor with LPDDR3

2017-06-05

REV1.0


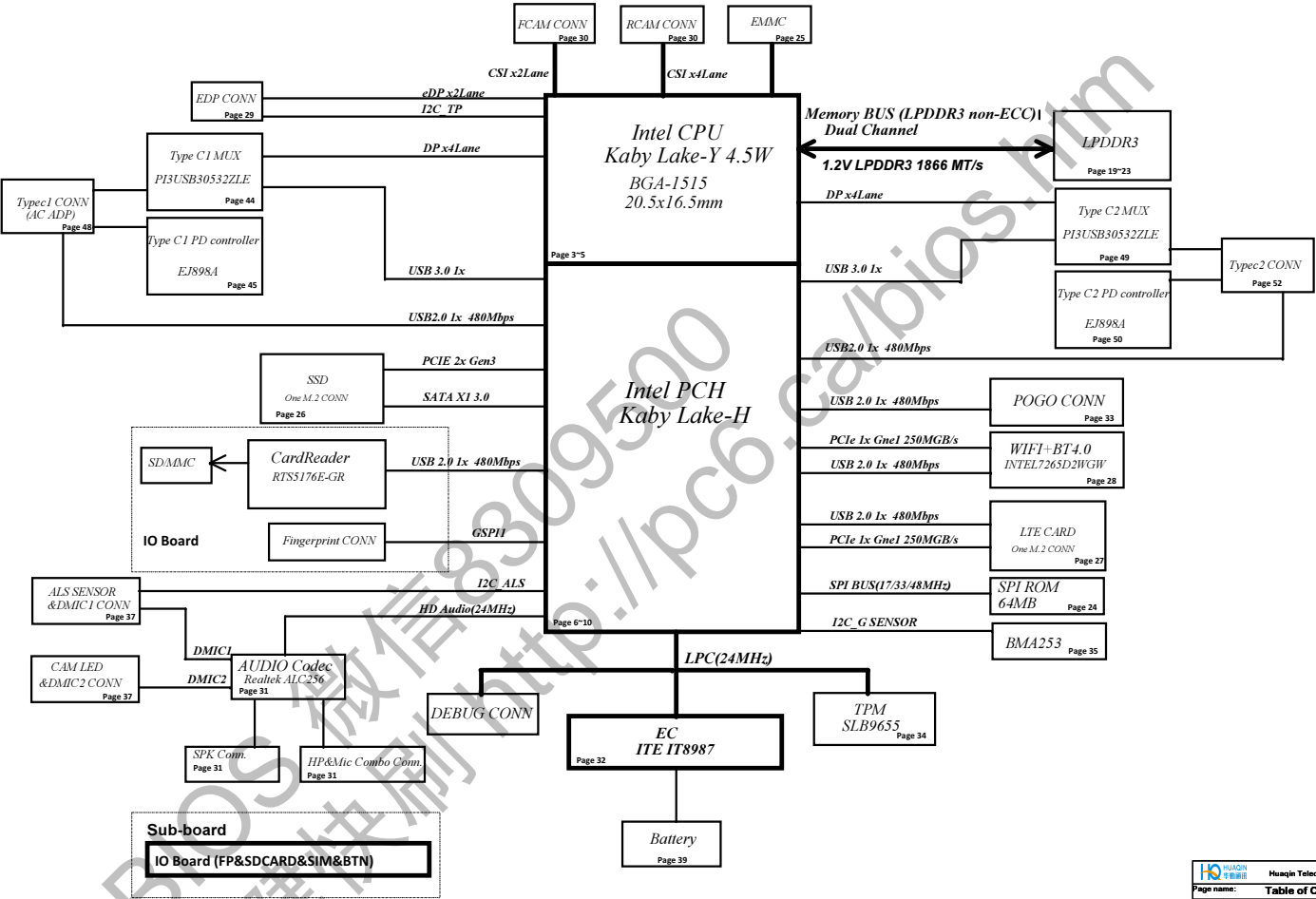
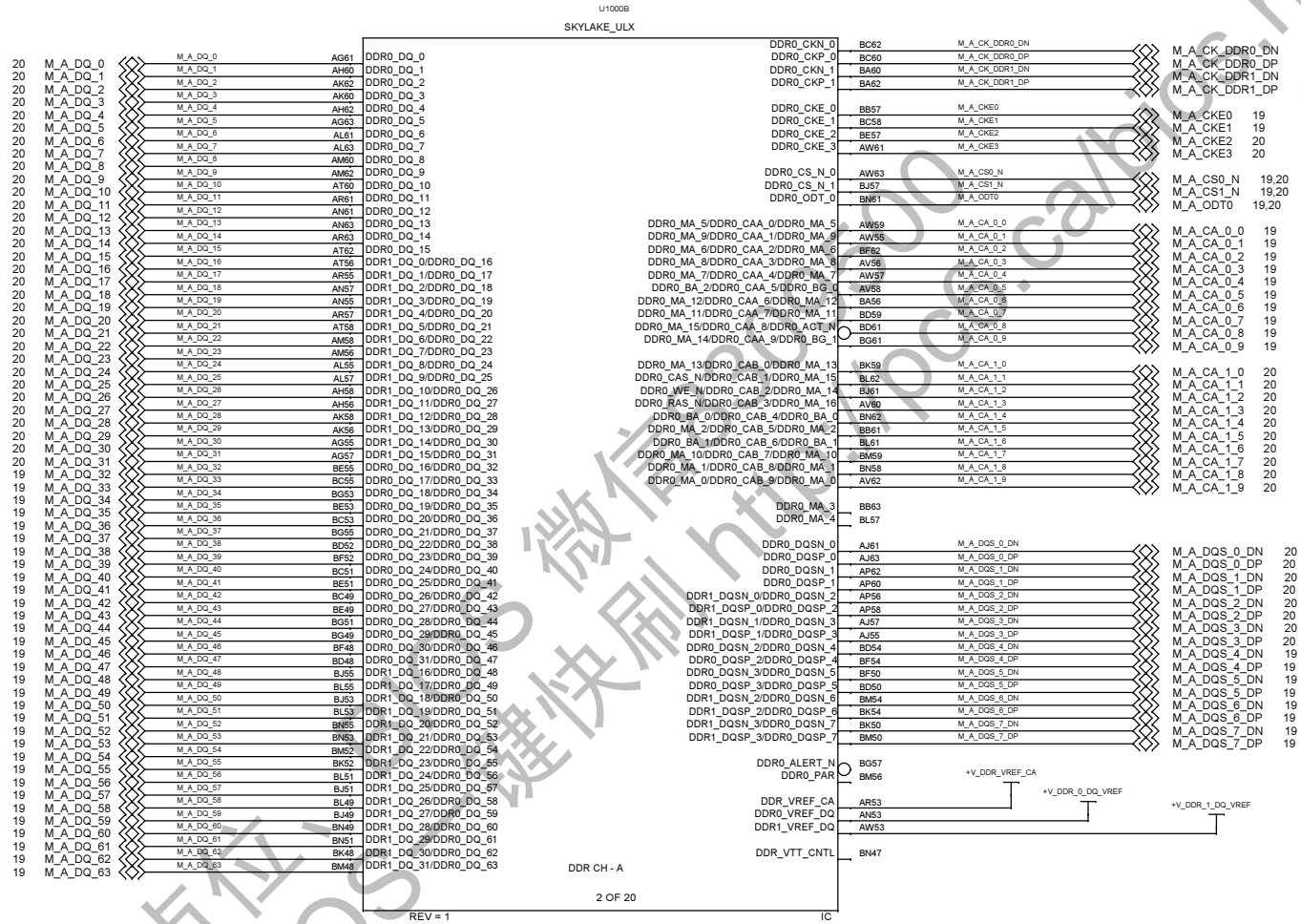
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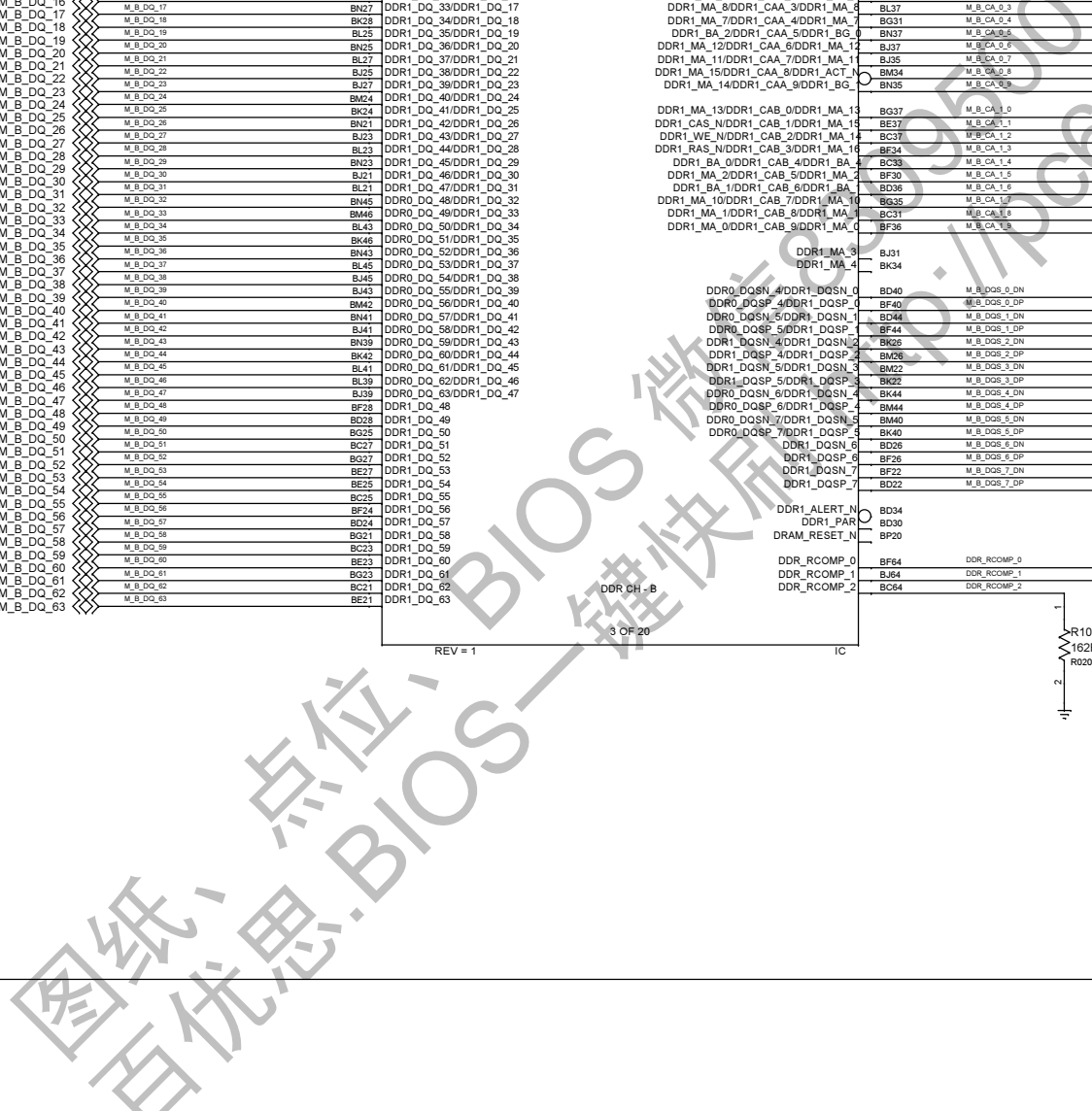
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36	HL SOC (DDR CHA)	76	TYPE C1 CARRIER MS
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38	HL SOC (DDR CHA)	78	TYPE C1 PD CONTROLLER
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40	HL SOC (DDR CHA)	80	TYPE C1 CARRIER MS

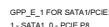


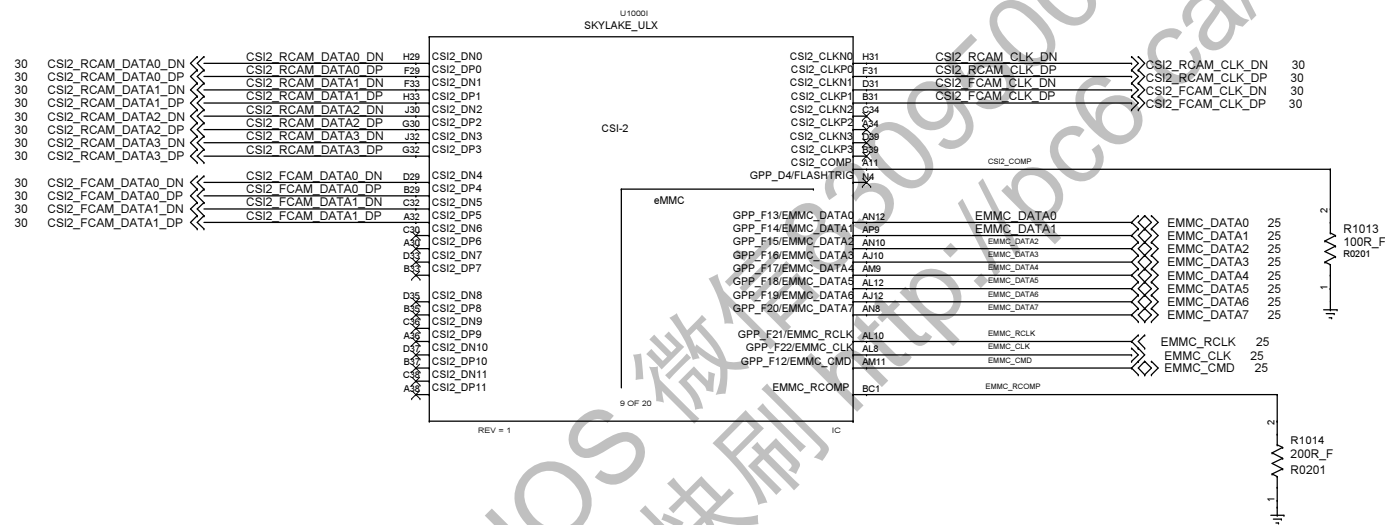
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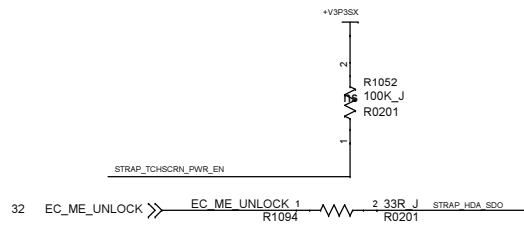




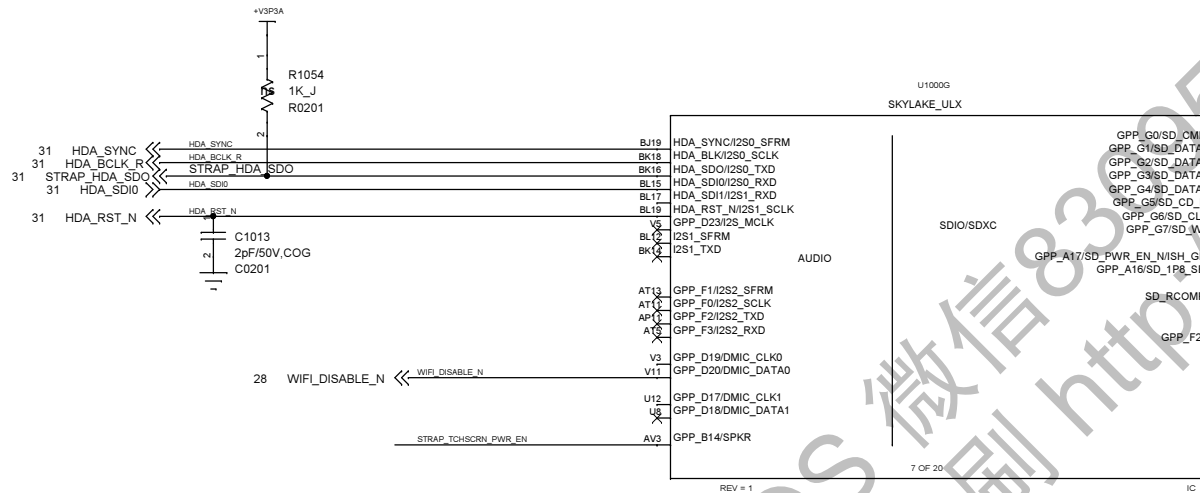







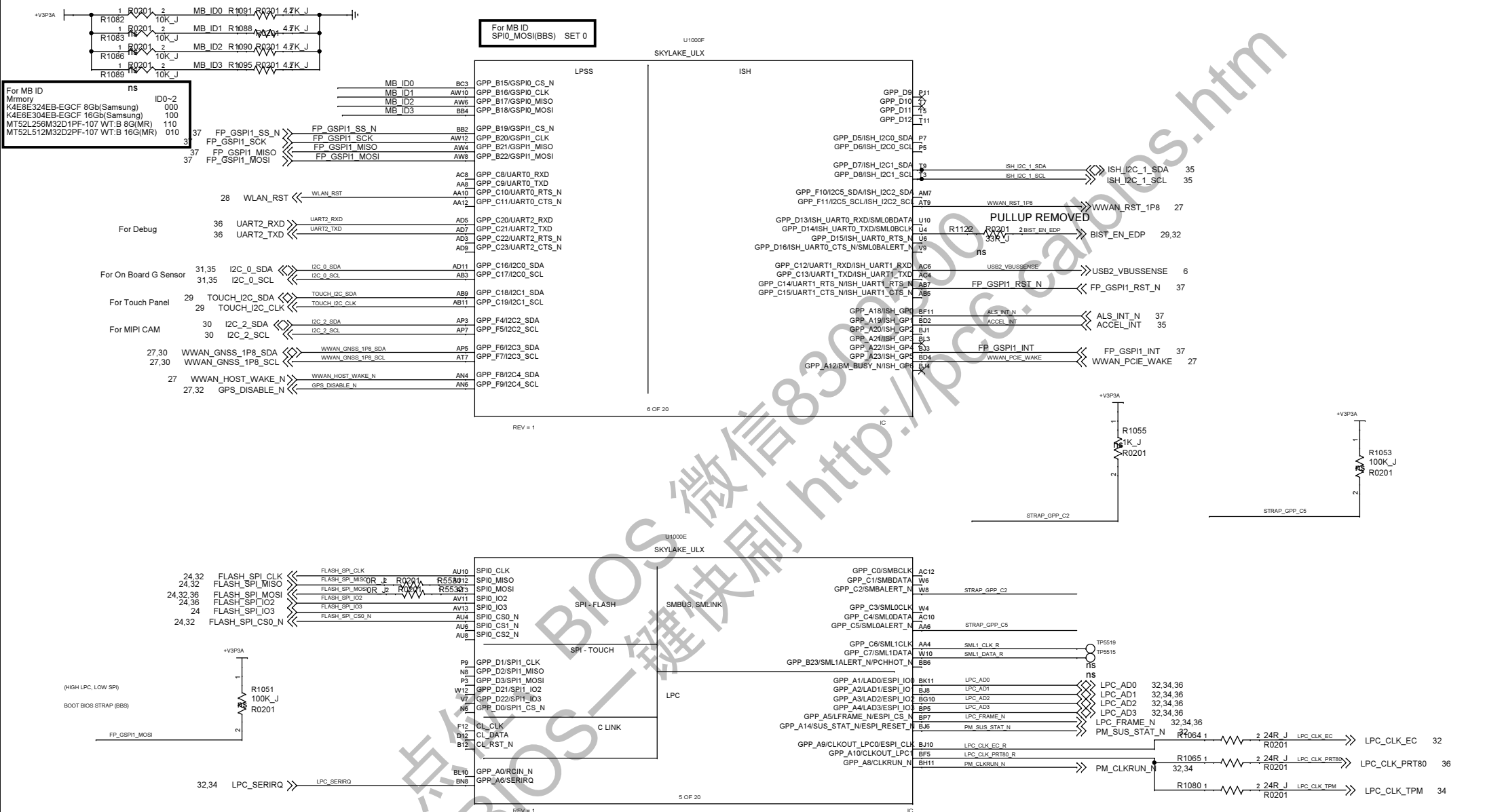


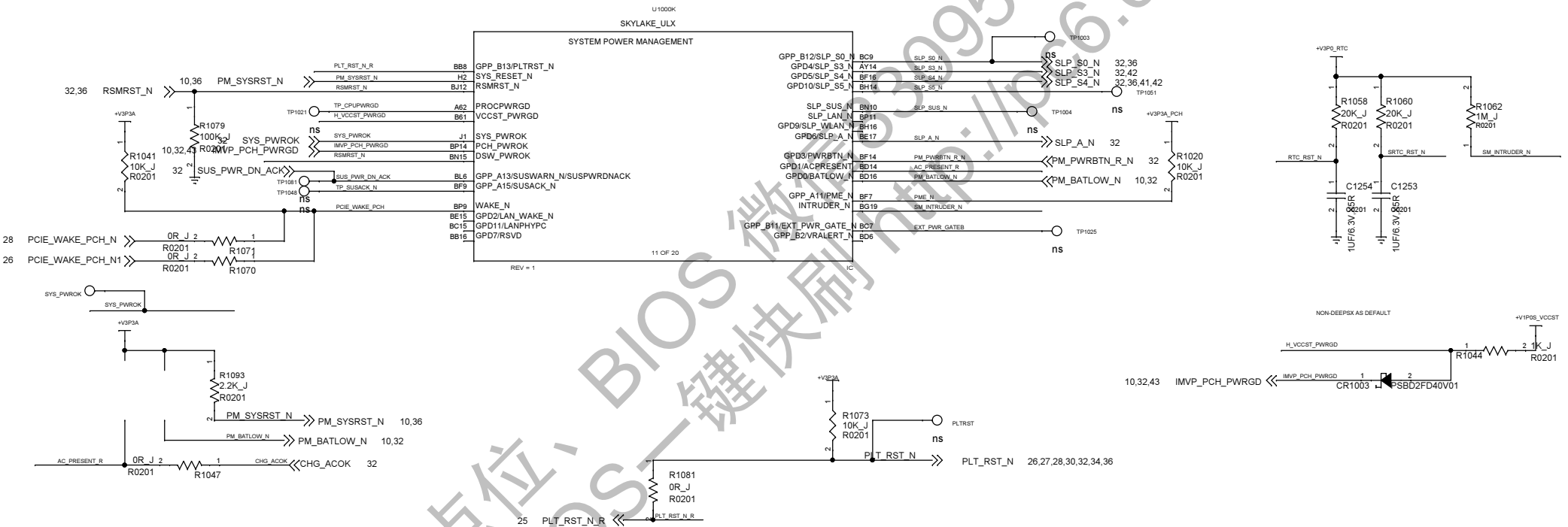
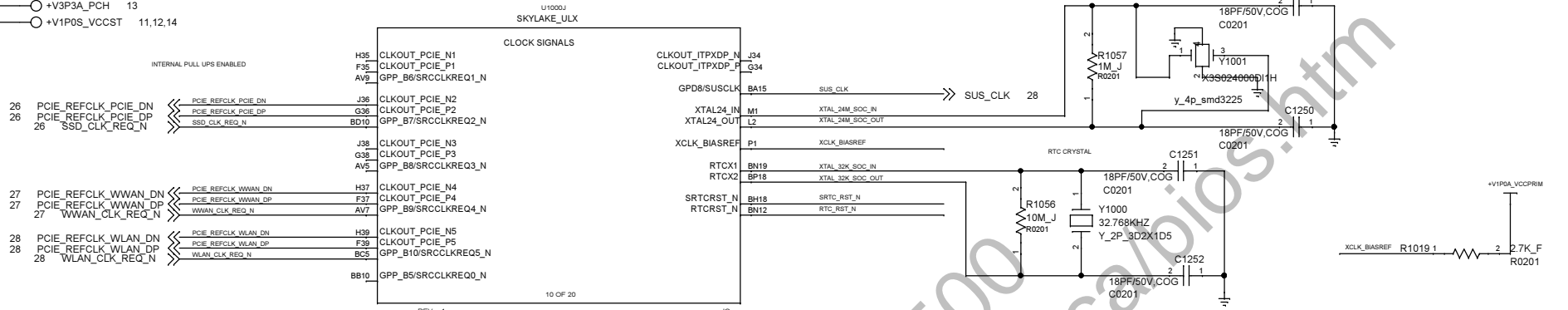
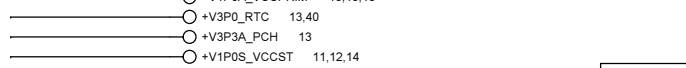
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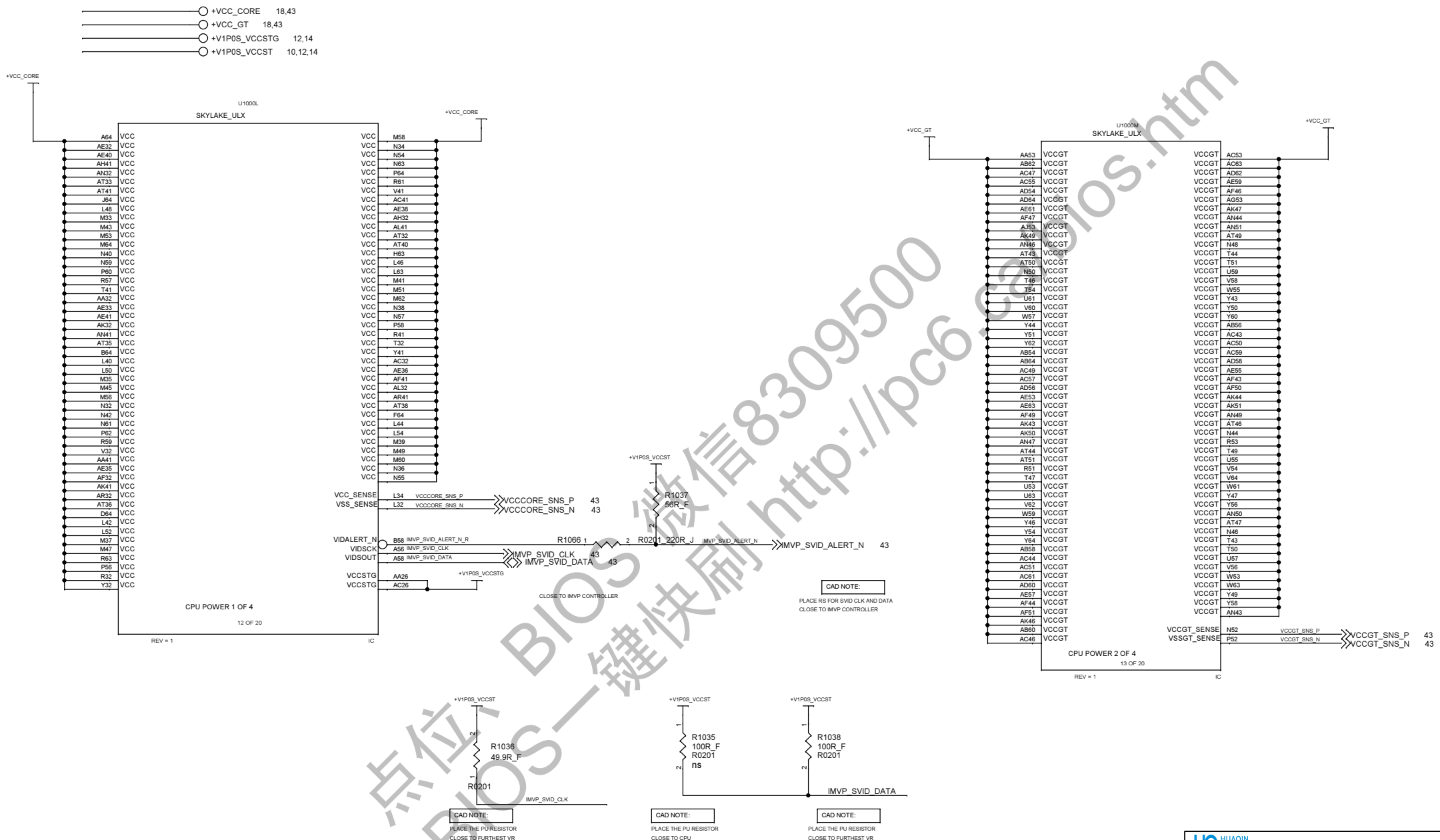


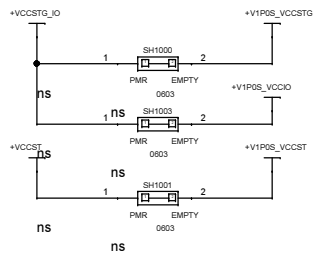
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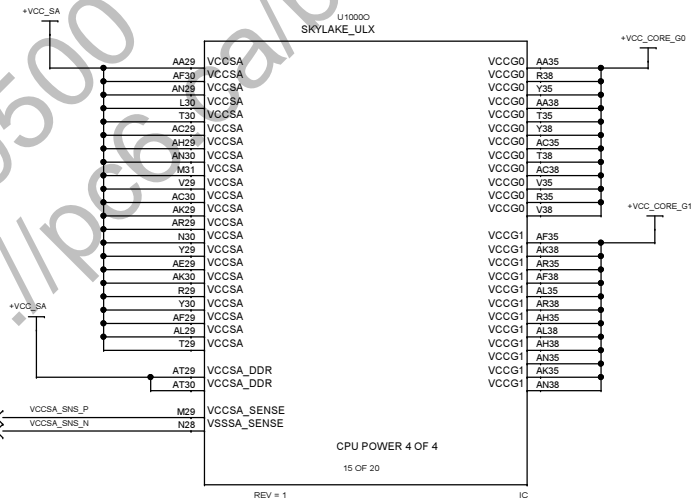
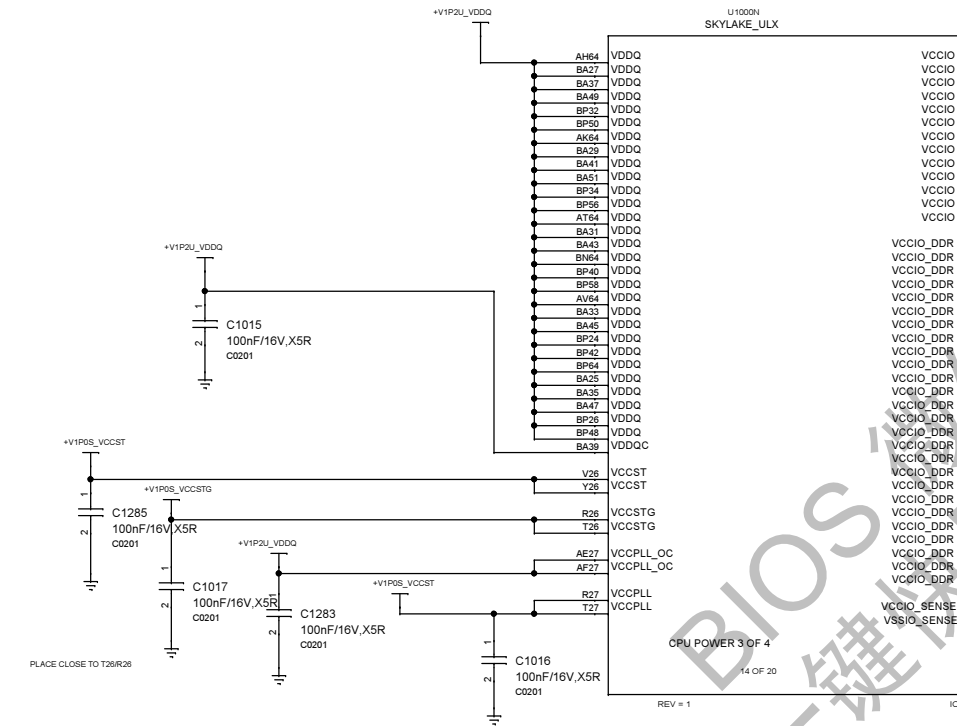




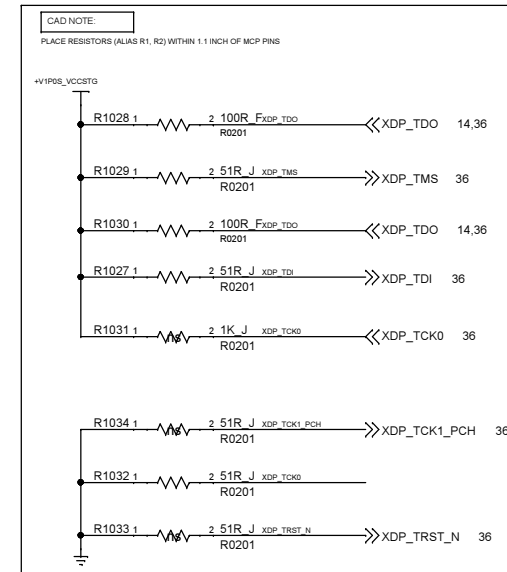
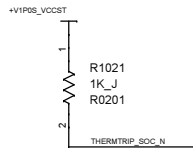
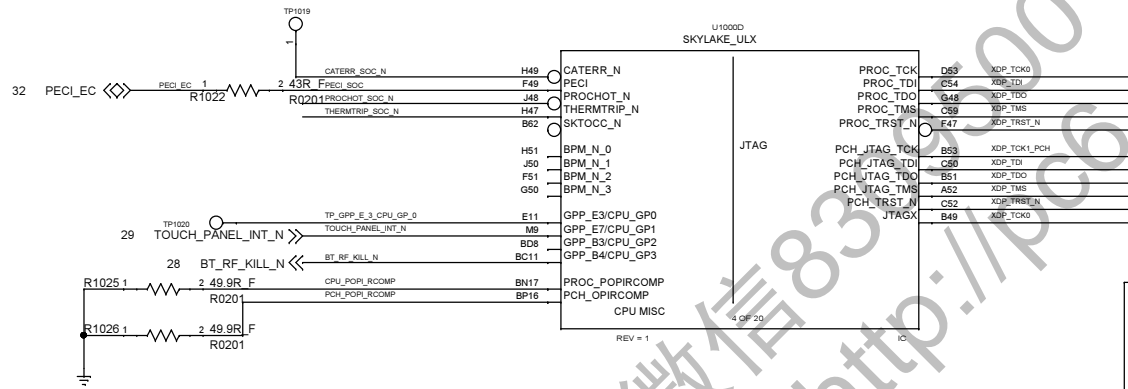




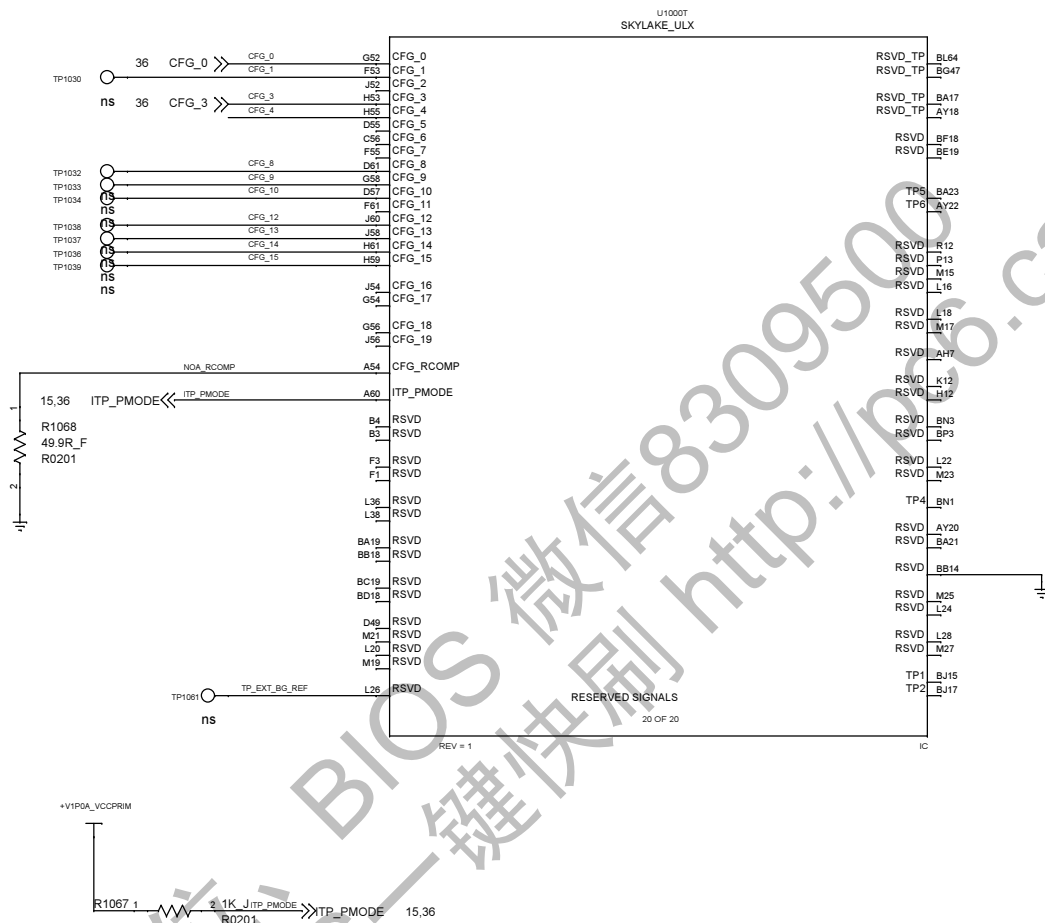
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+VCCST	42
+V1P0S_VCCSTG	11,14
+V1P0S_VCCIO	5,17
+V1P0S_VCCST	10,11,14
+V1P2U_VDDQ	17,19,20,21,22,23,41
+VCC_SA	17,43
+VCC_CORE_G0	17
+VCC_CORE_G1	17



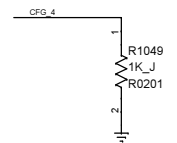




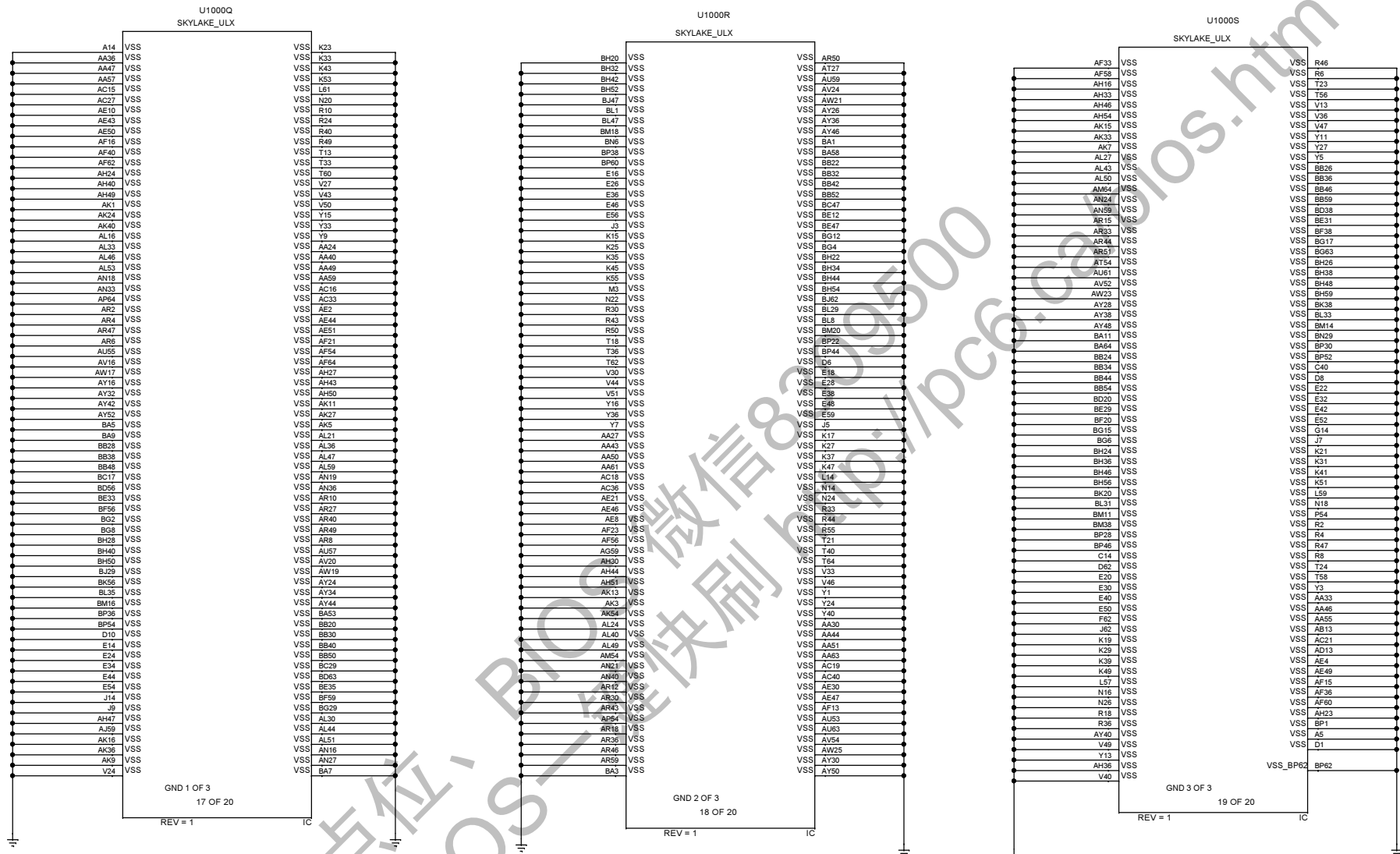
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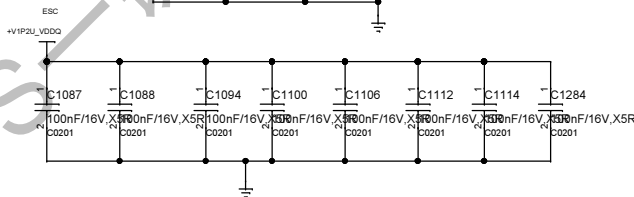
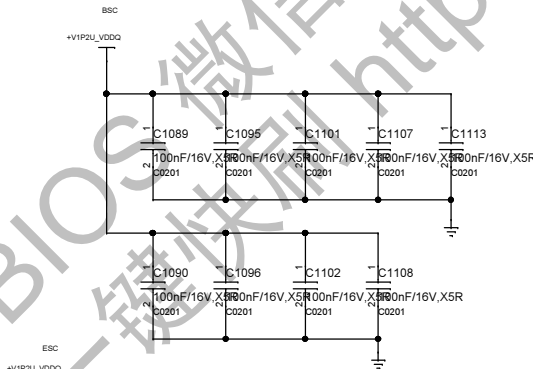
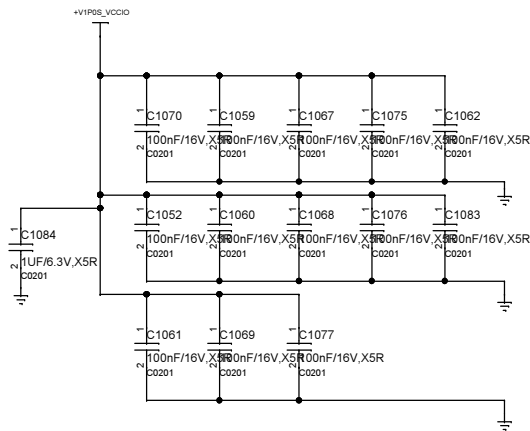
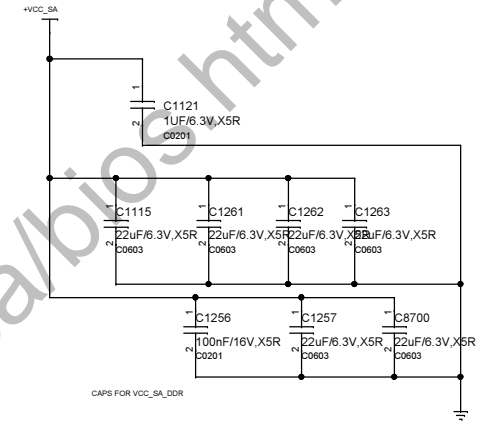
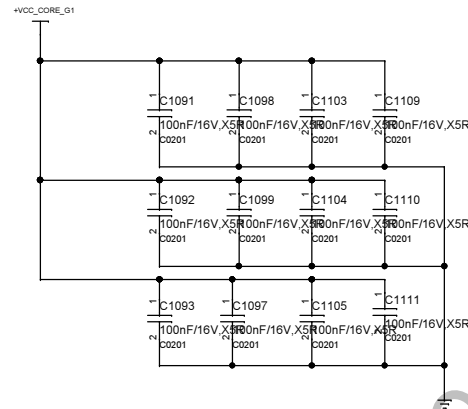
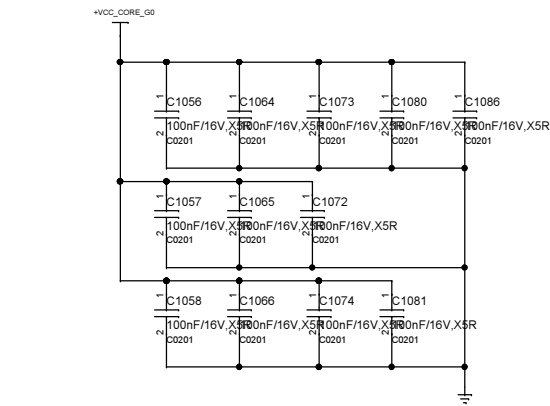
DISPLAY PORT PRESENCE STRAP  
0 (DEF) ENABLED  
EXT DP DEV IS CONNECTED TO  
EMBEDDED DISPLAY PORT  
1: DISABLED  
NO DP DEV ATTACHED TO  
EMBEDDED DISPLAY PORT




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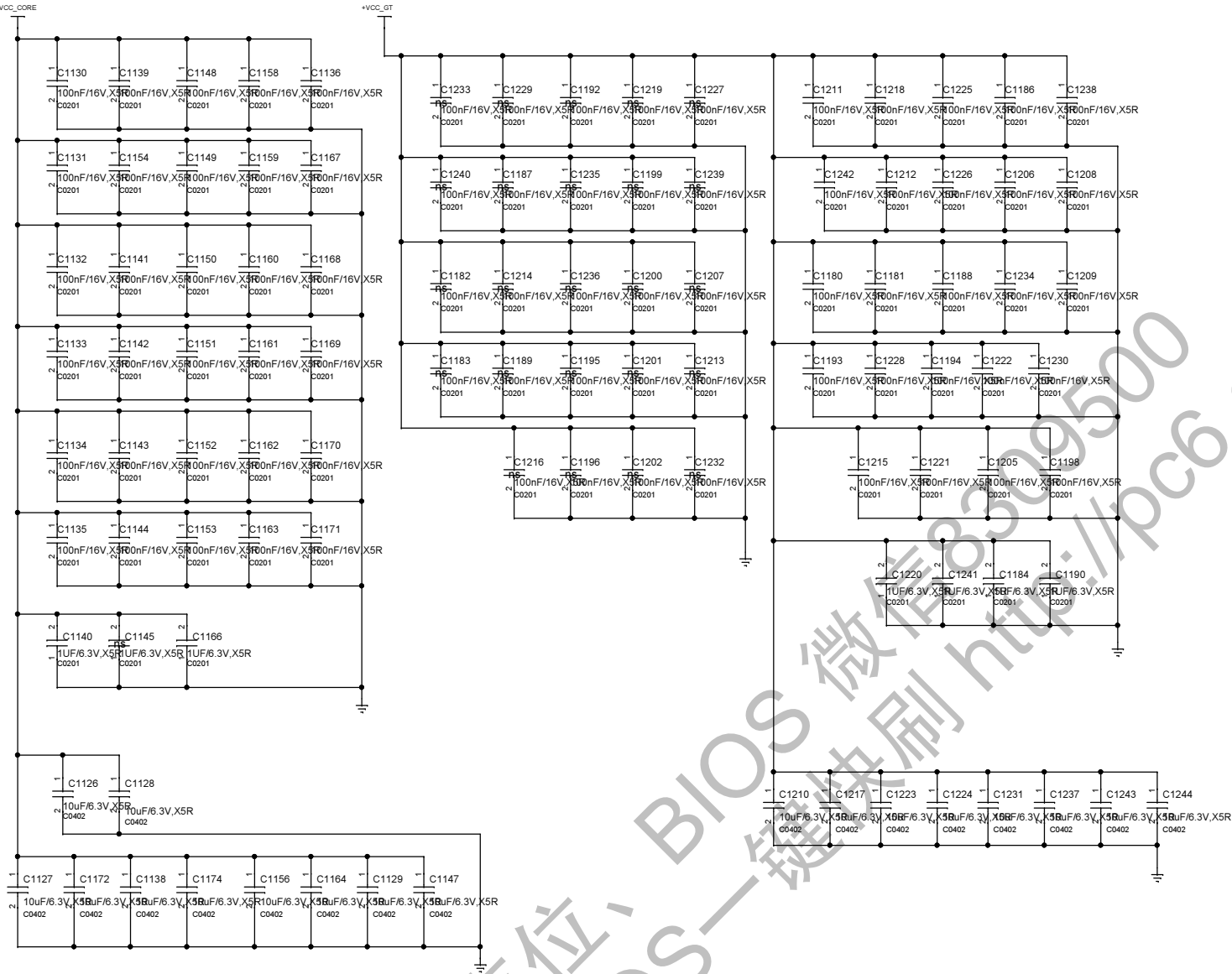




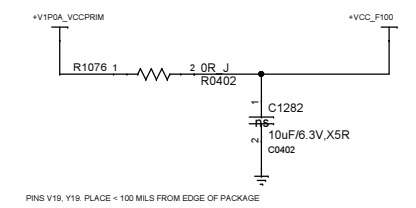
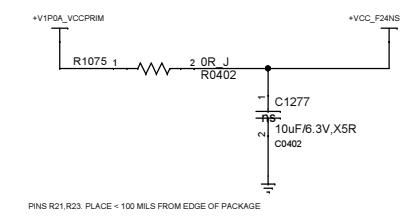
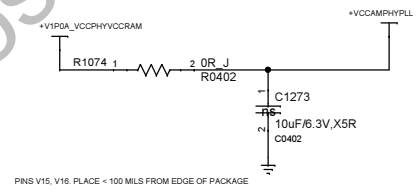


- +VCC\_CORE\_G0 12
- +VCC\_CORE\_G1 12
- +VCC\_SA 12,43
- +V1P0S\_VCCIO 5,12
- +V1P2U\_VDDQ 12,19,20,21,22,23,41

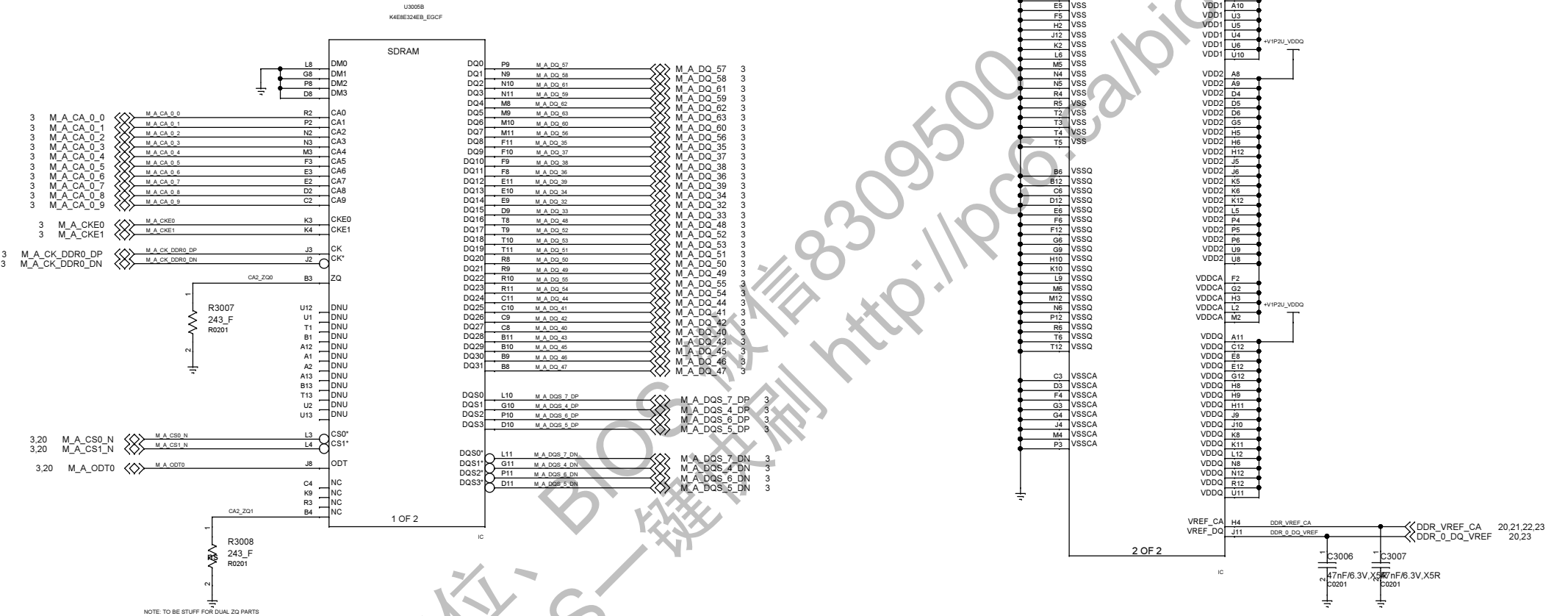
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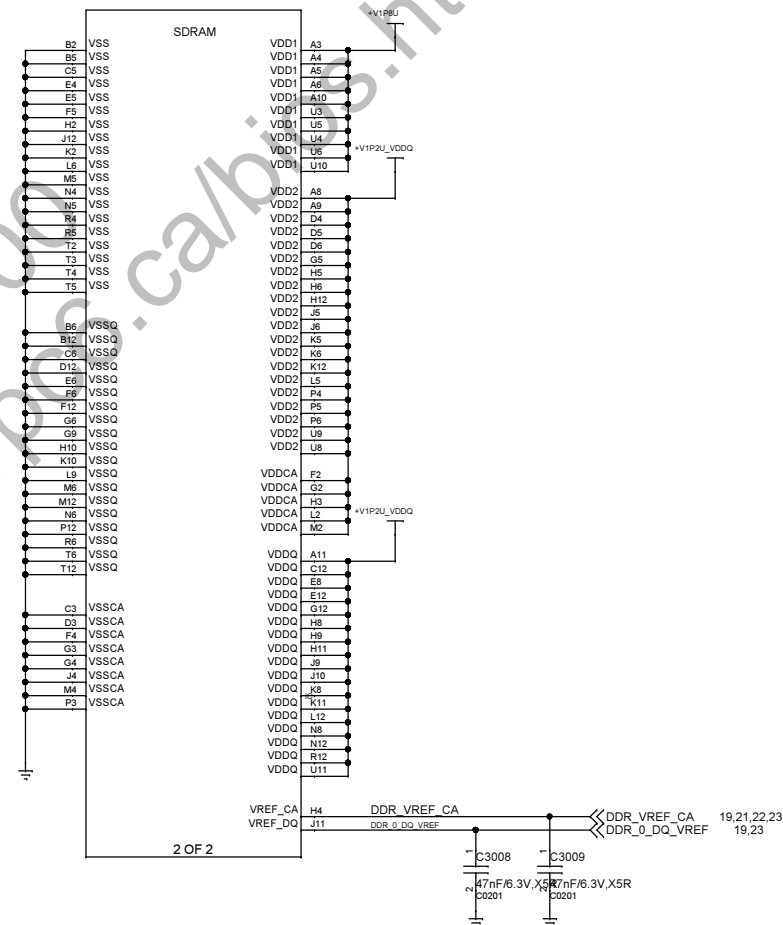
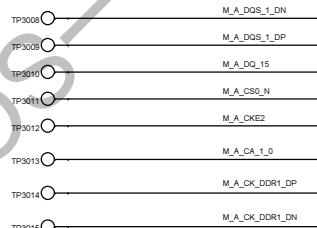


- +VCC\_CORE 11,43
- +VCC\_GT 11,43
- +V1P0A\_VCCPHYVCCRAM 13
- +VCCAMPHYPLL 13
- +V1P0A\_VCCPRIM 10,13,15
- +VCC\_F24NS 13
- +VCC\_F100 13



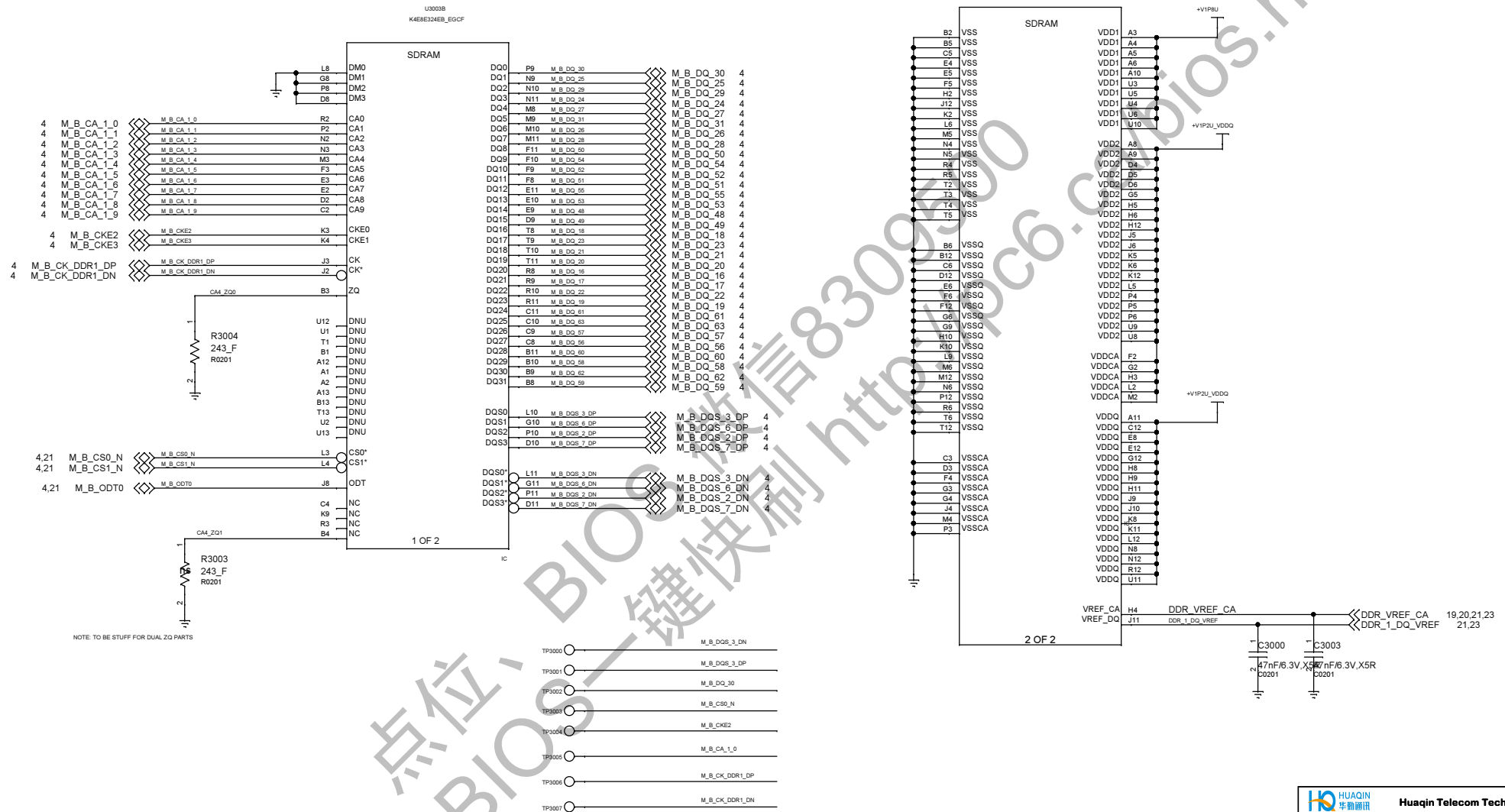
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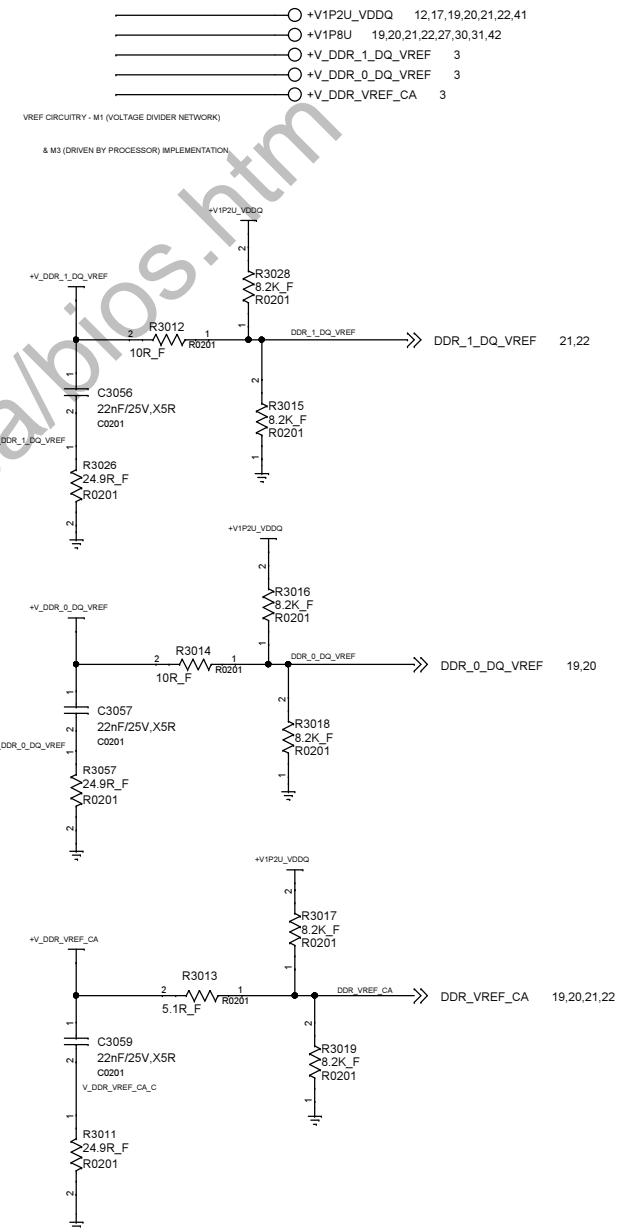
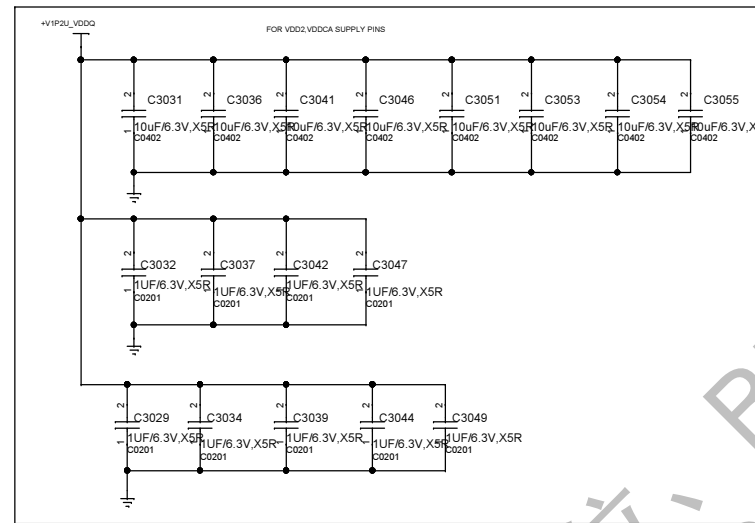
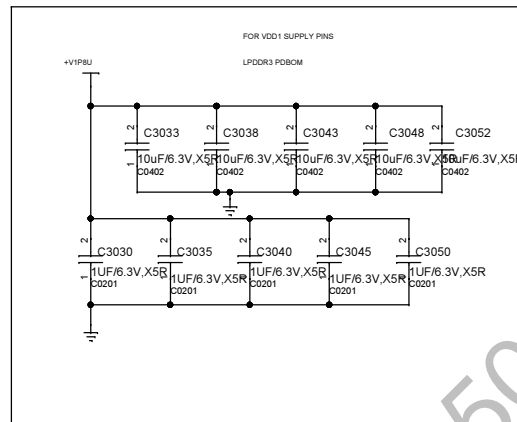
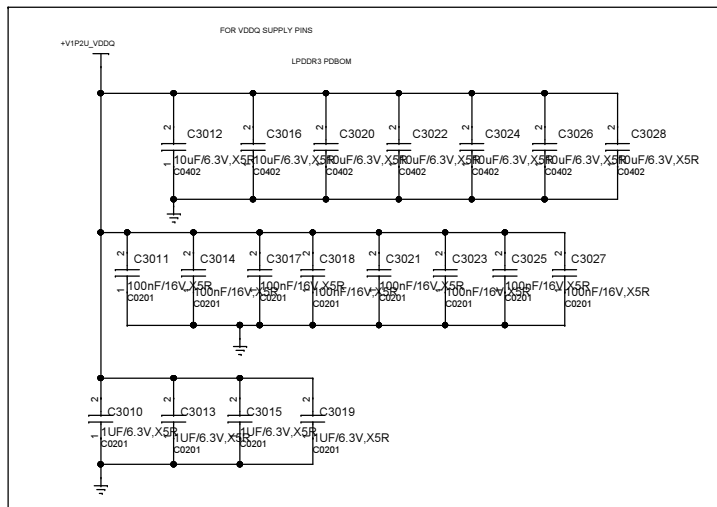






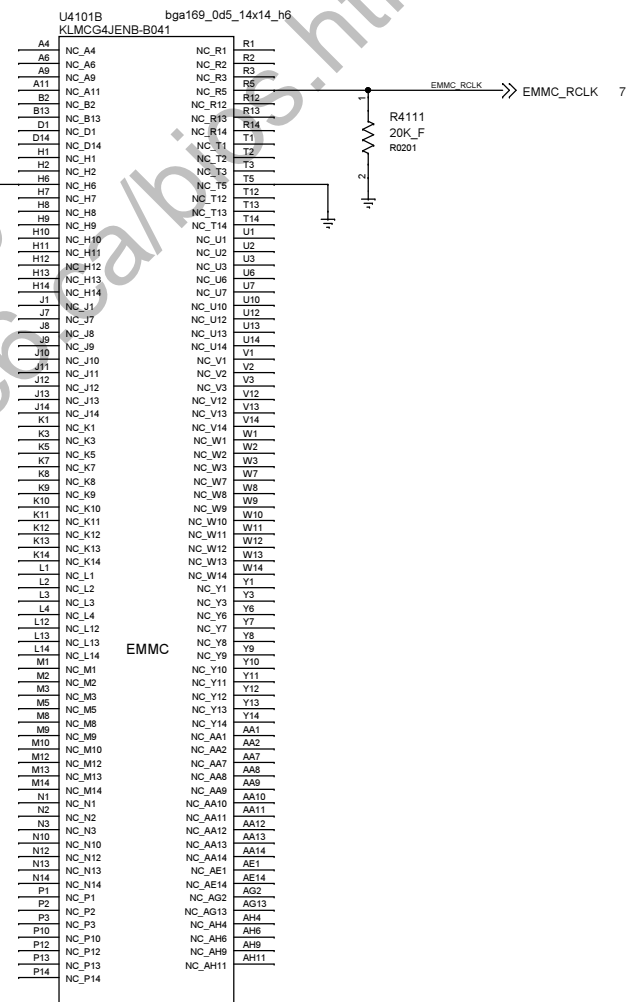
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+V1P8U 19,20,21,23,27,30,31,42

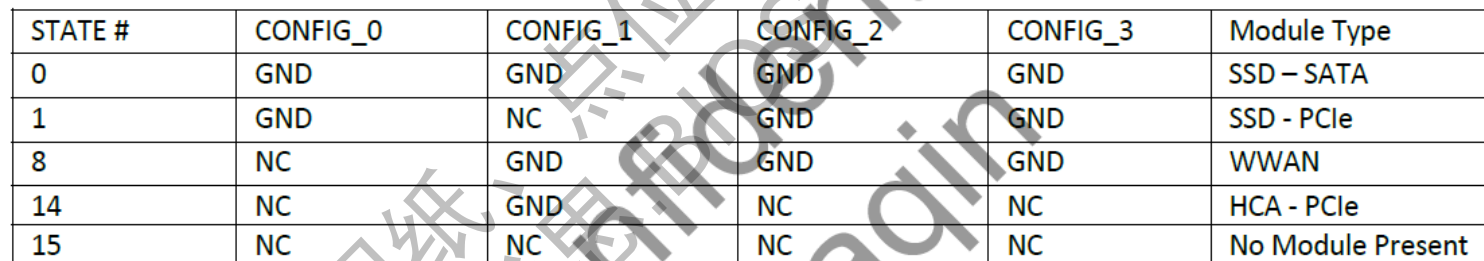
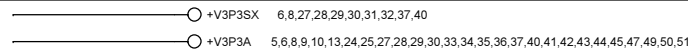




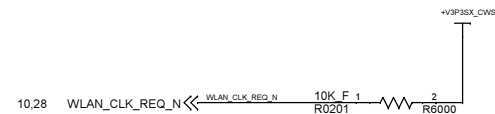
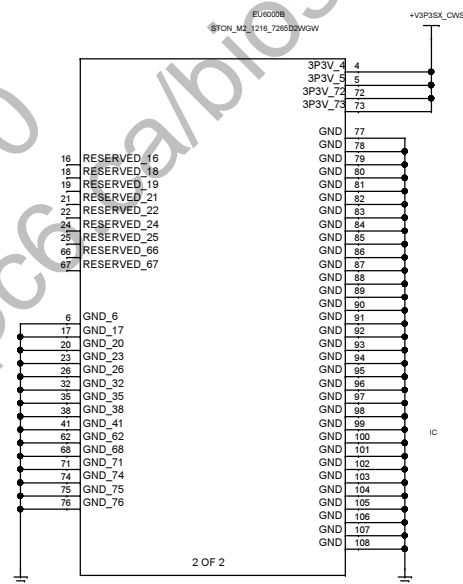
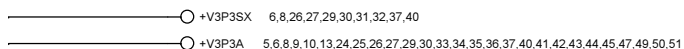










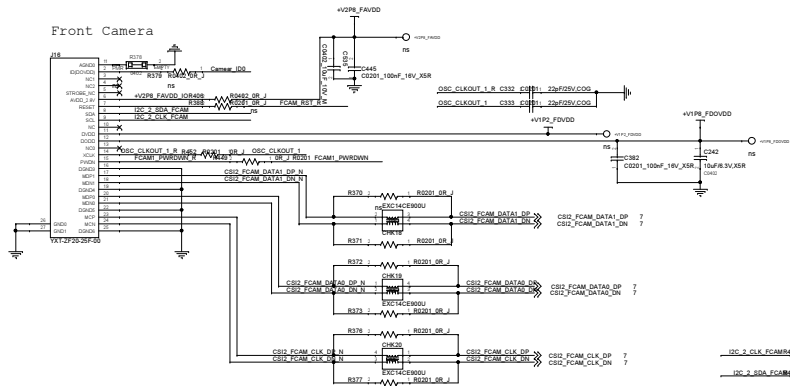




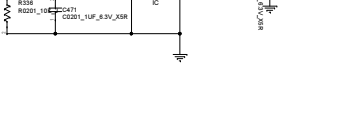
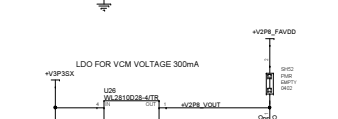
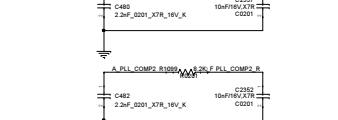
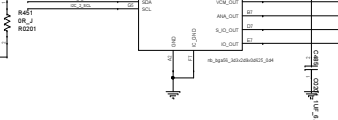
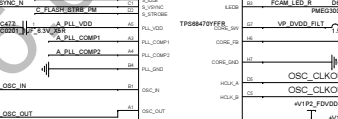
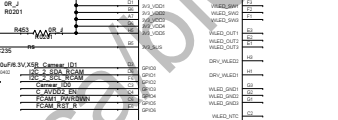
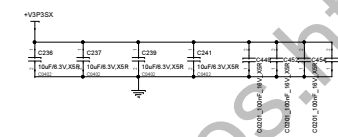
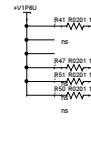
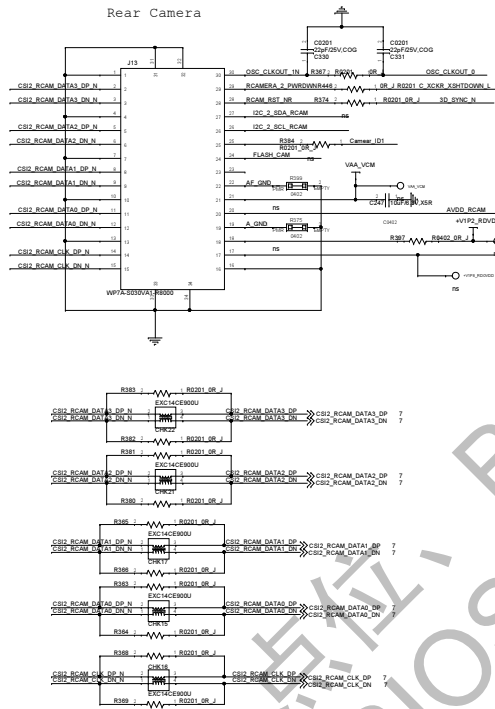
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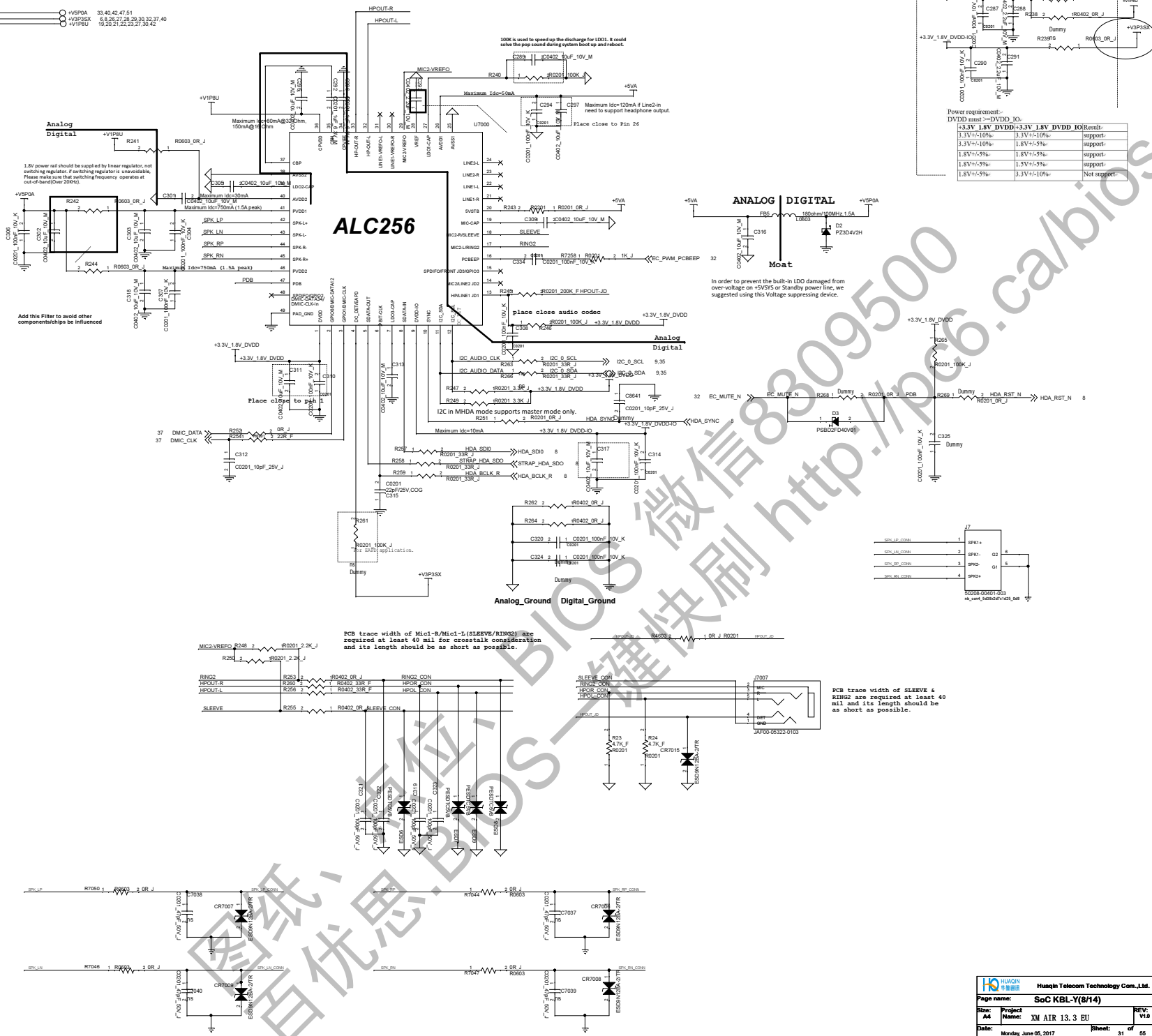
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## Front Camera

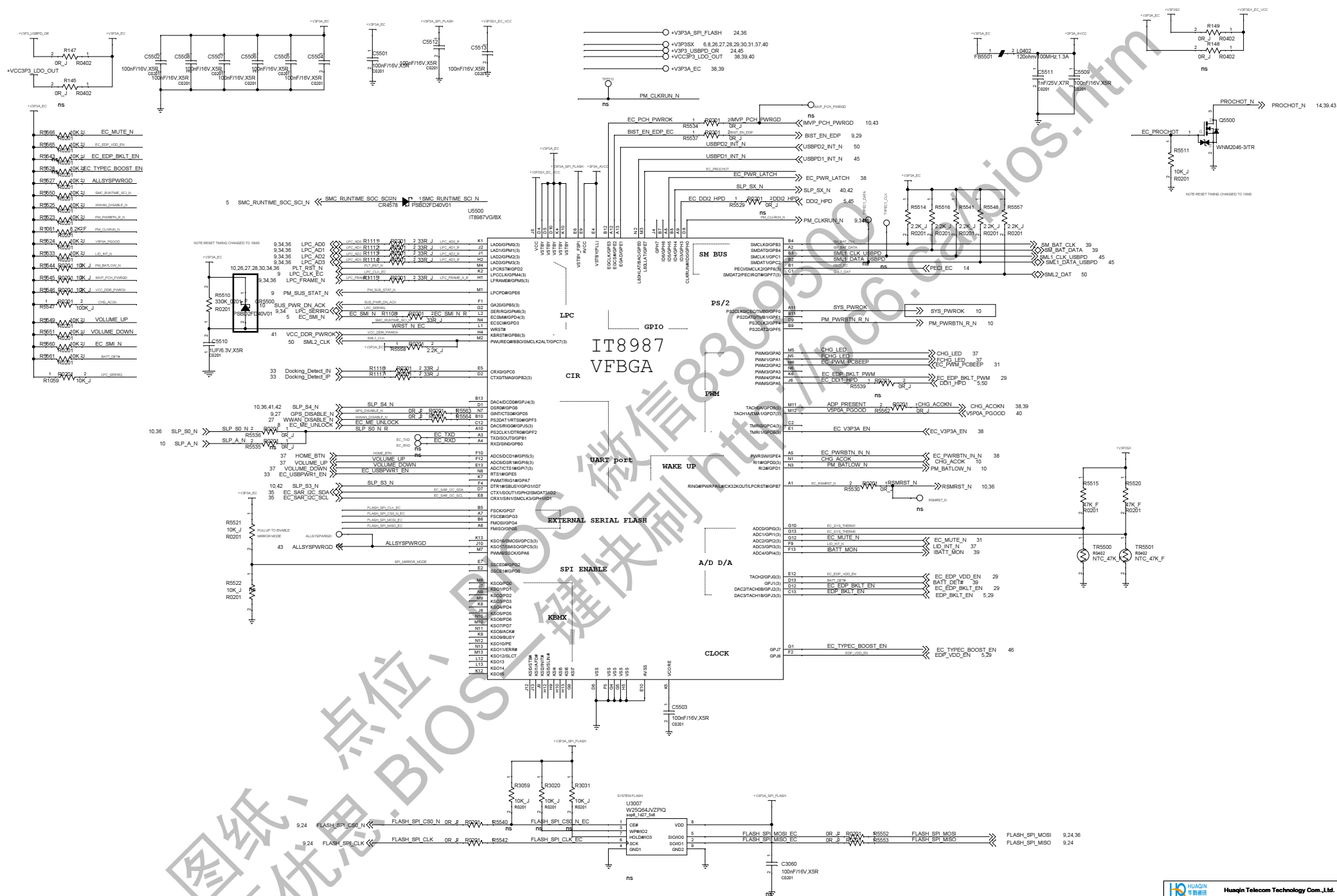


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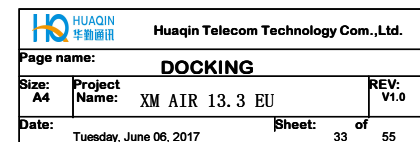




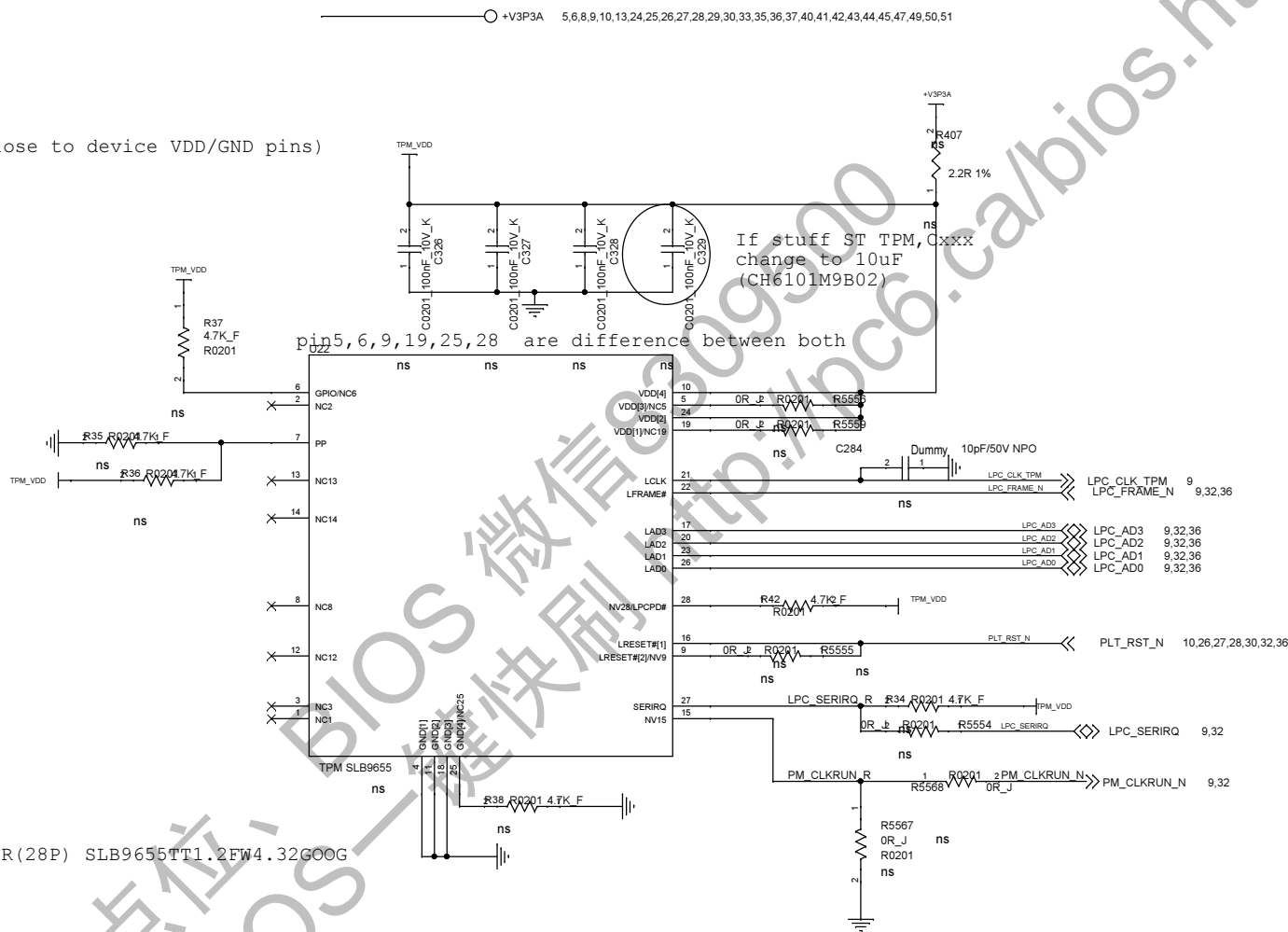








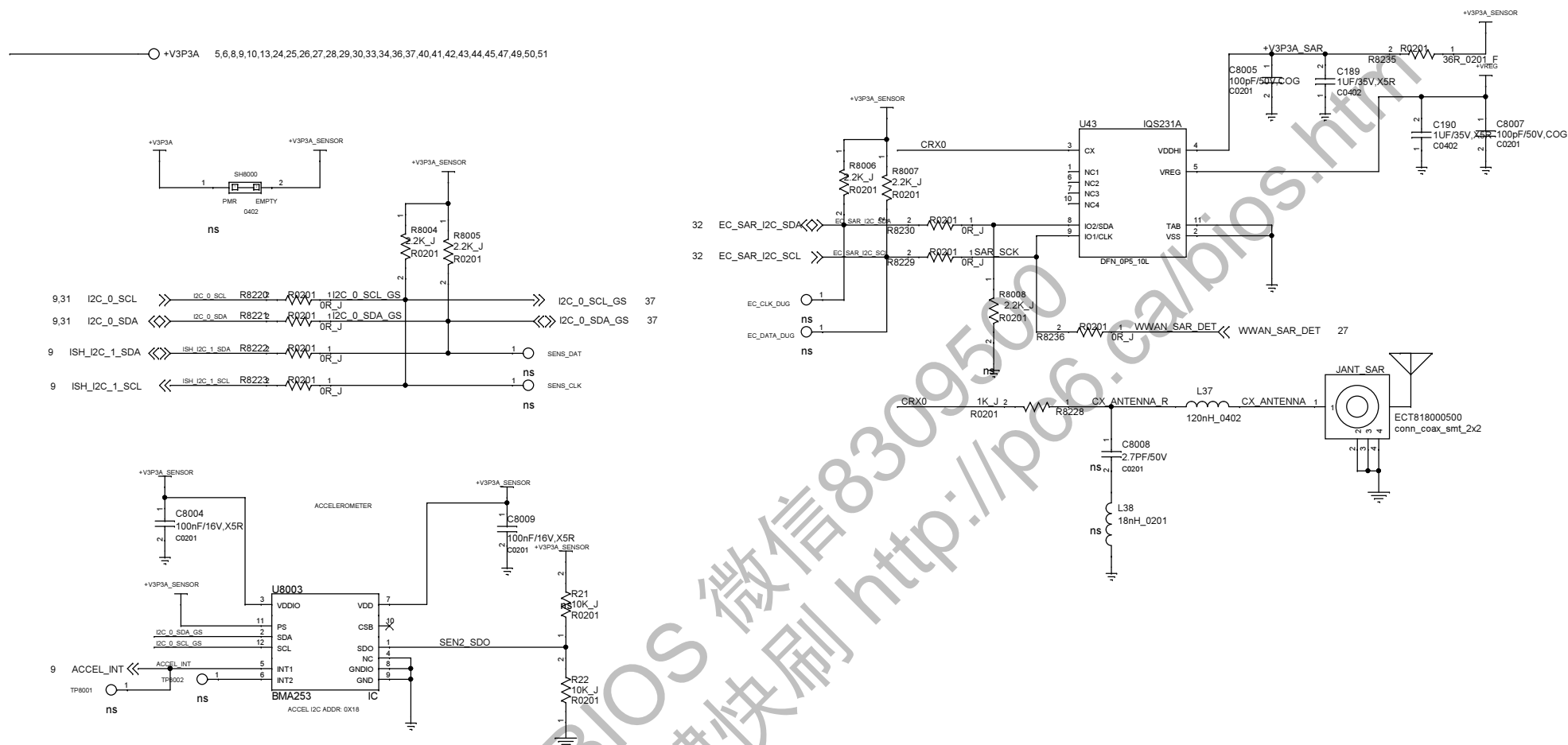
4x100nF  
(Place close to device VDD/GND pins)



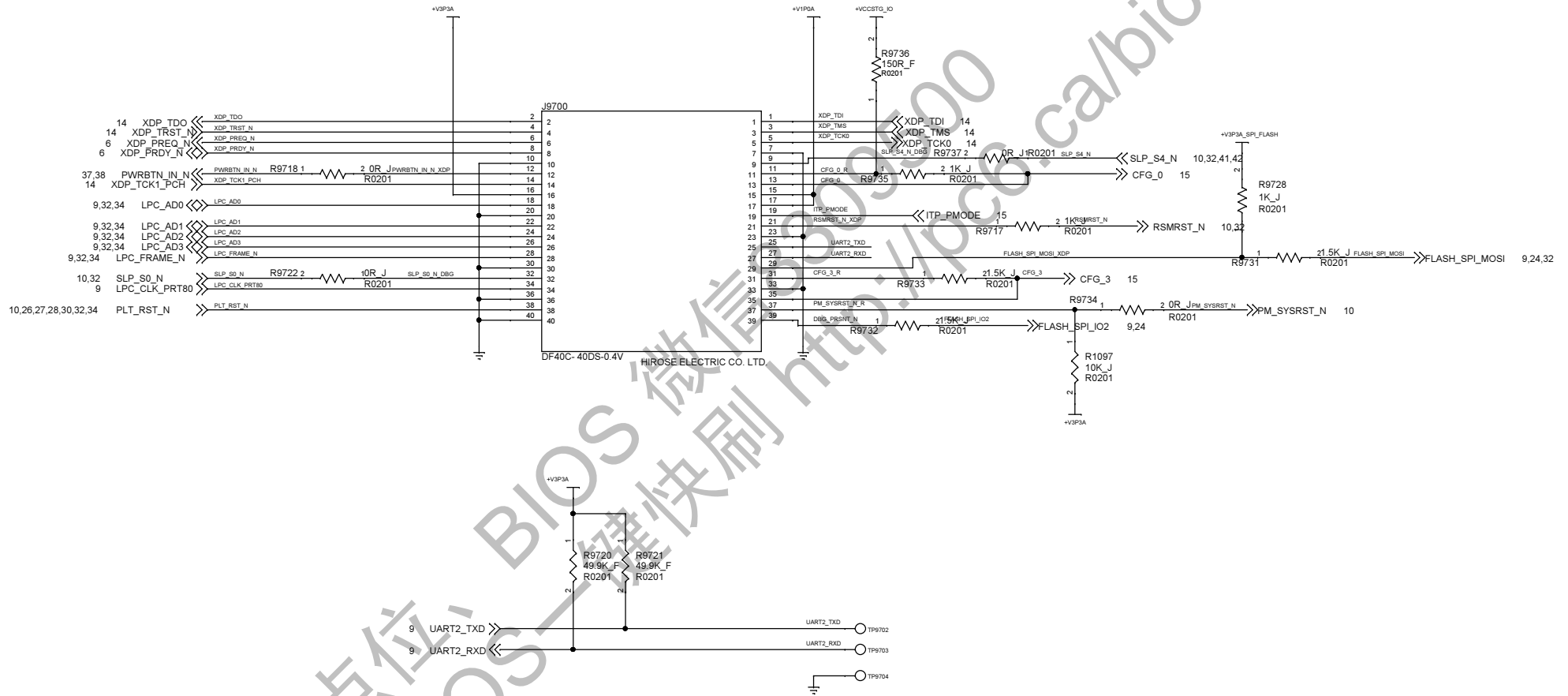
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Note: R156:ILED=1000/49.9K=20mA.

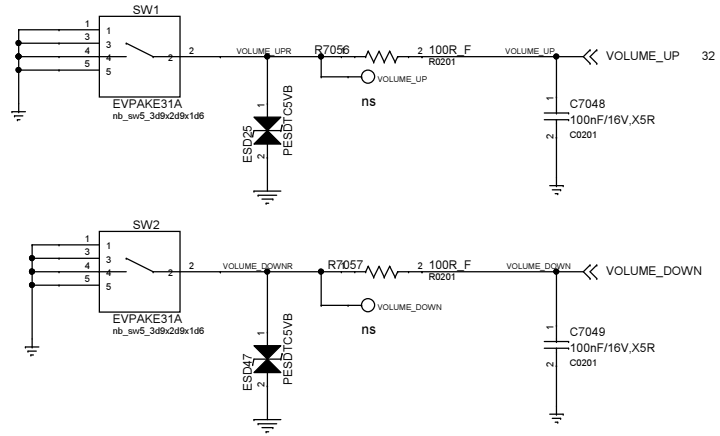
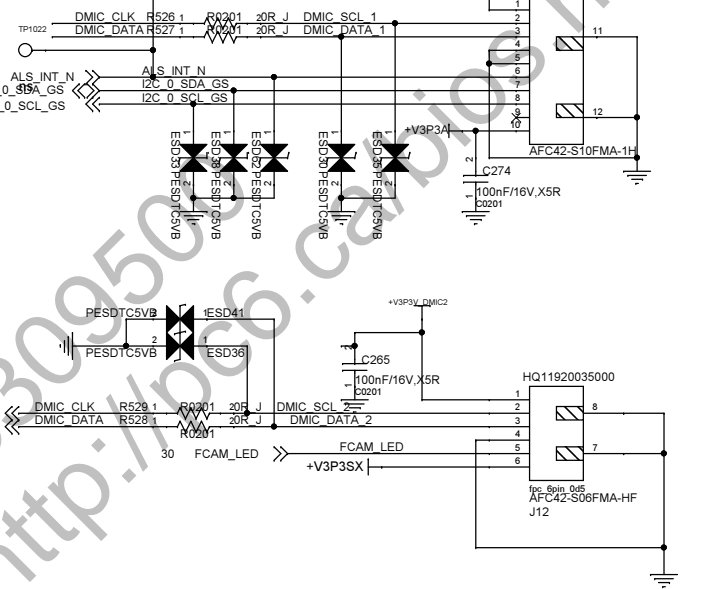
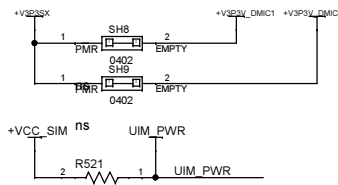
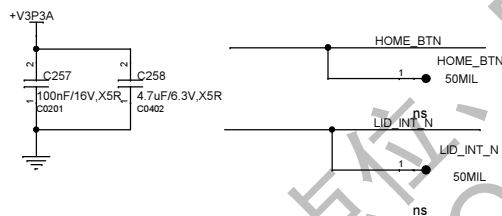
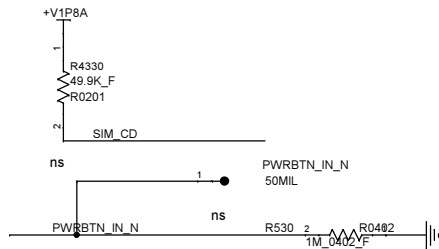
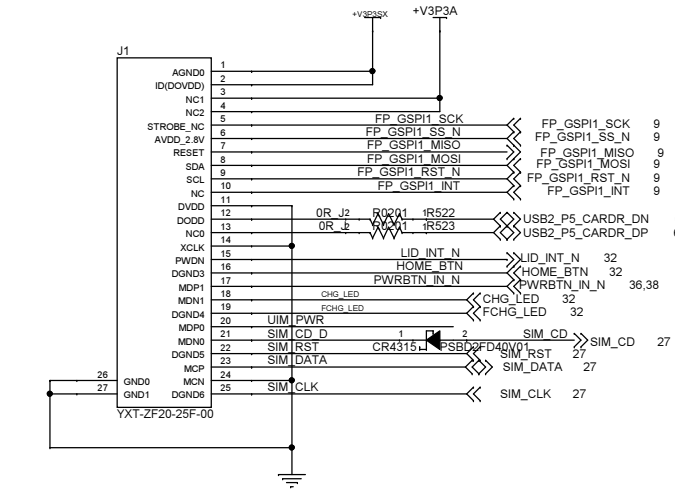
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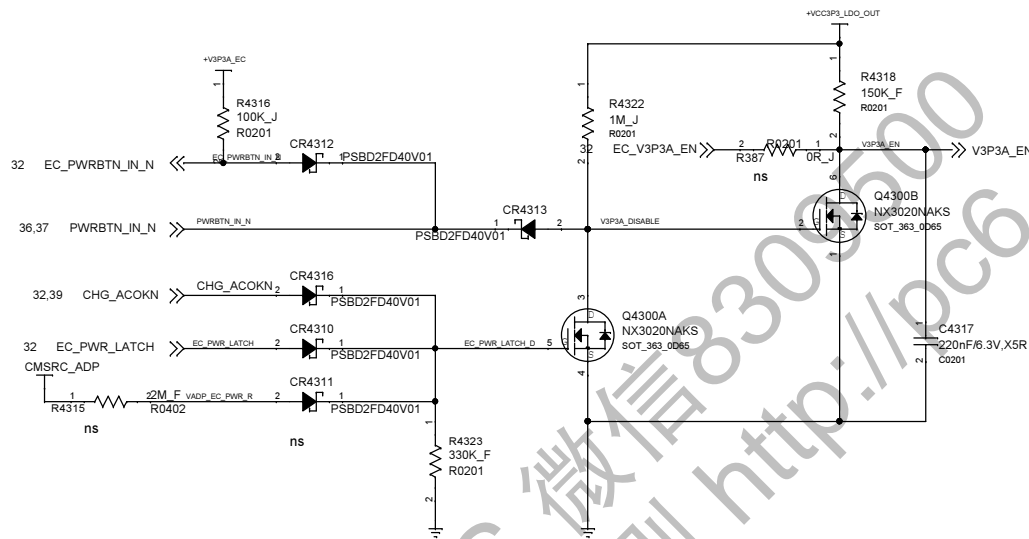
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+V1P0A 13,42  
+VCCSTG\_IO 12,42  
+V3P3A\_SPI\_FLASH 24,32




+V3P3SX 6,8,26,27,28,29,30,31,32,40  
 +V3P3A 5,6,8,9,10,13,24,25,26,27,28,29,30,33,34,35,36,40,41,42,43,44,45,47,49,50,51  
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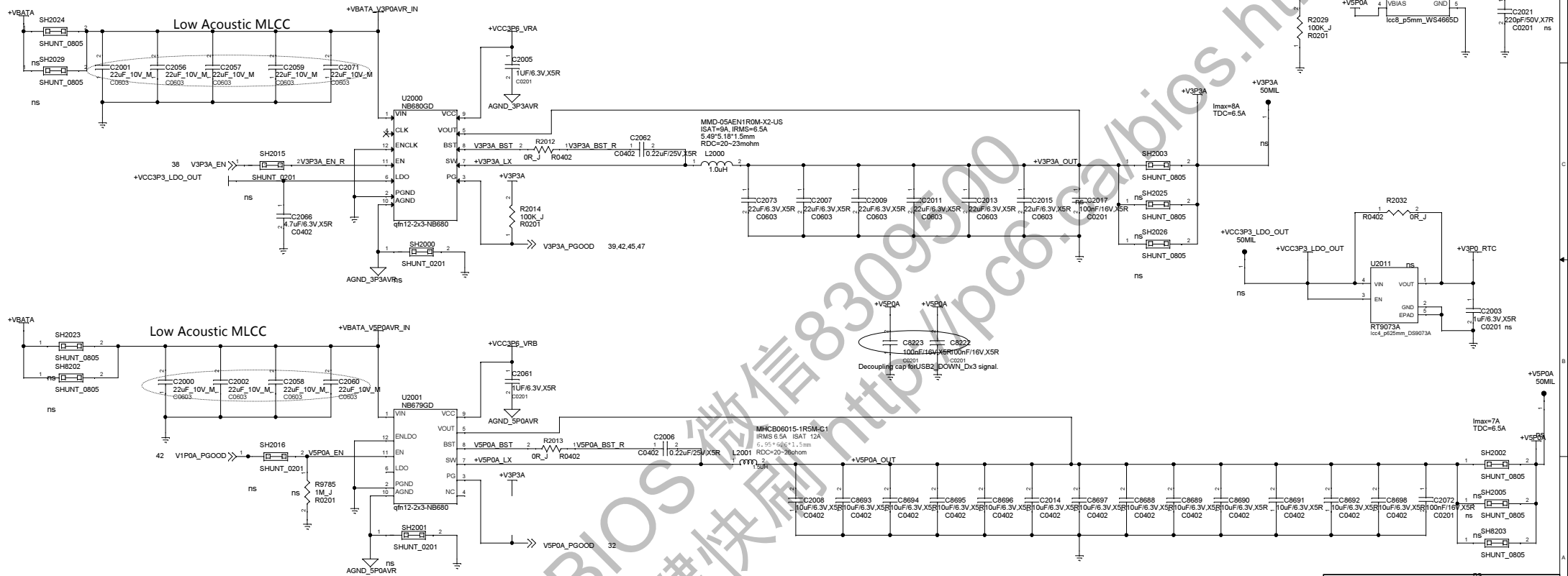
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○ +V3P3A\_EC 32,39  
○ CMSRC\_ADP 39




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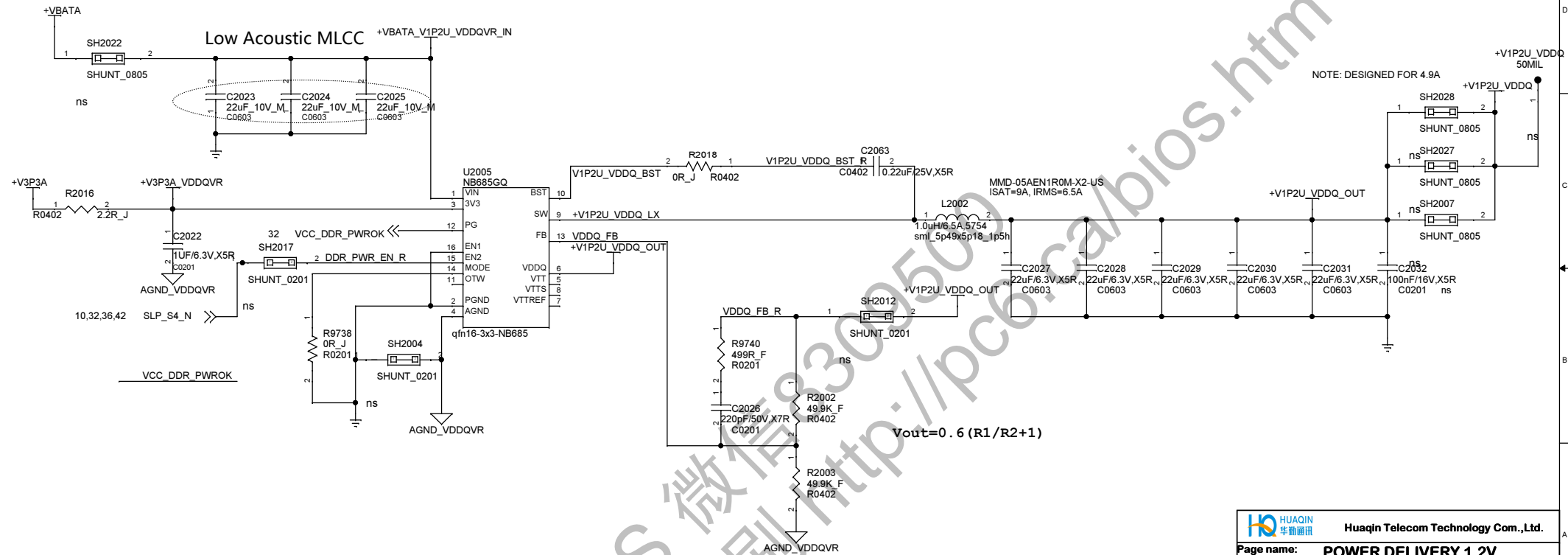
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+VCC3P3\_LDO\_OUT 32,38,39




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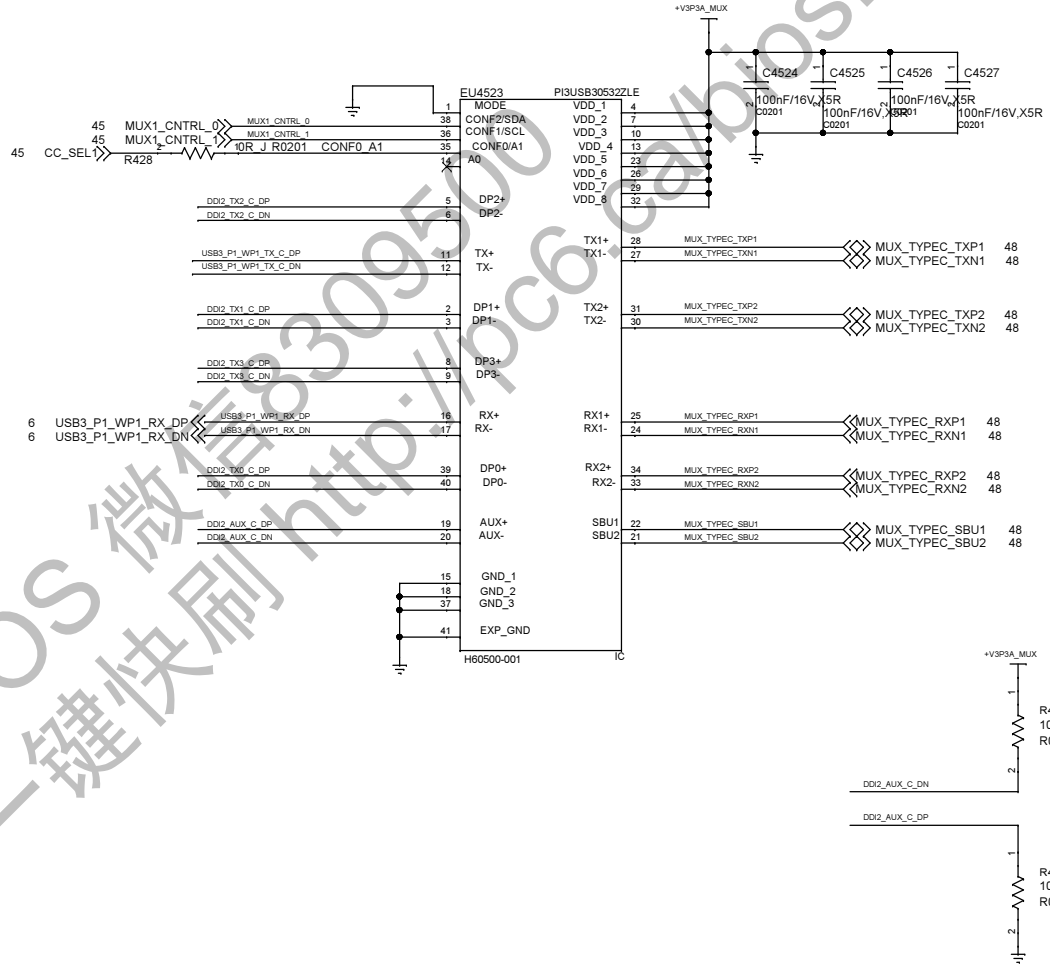
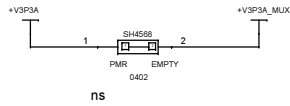
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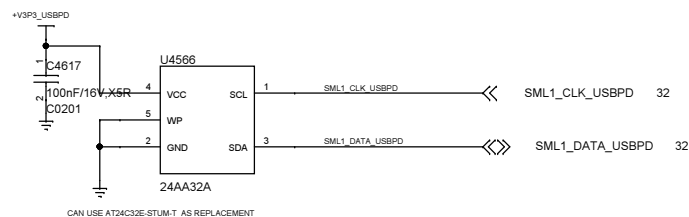
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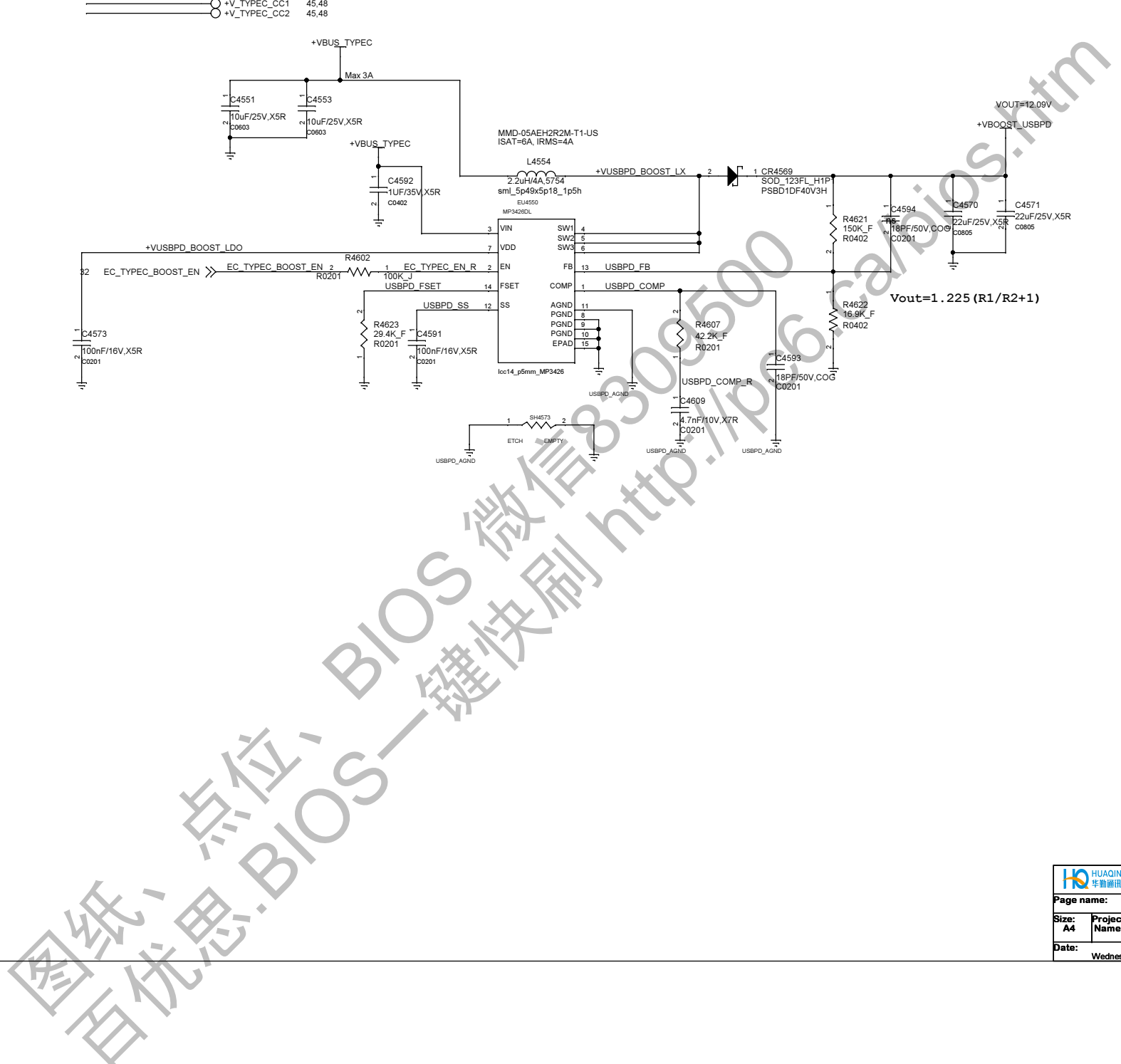




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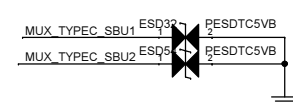
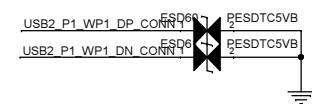
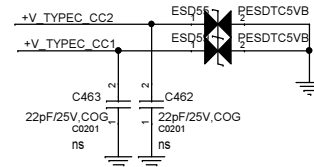
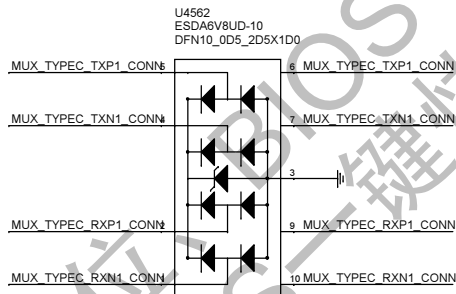
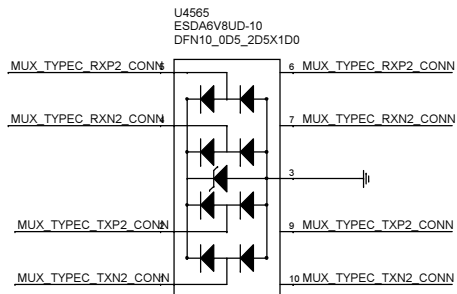
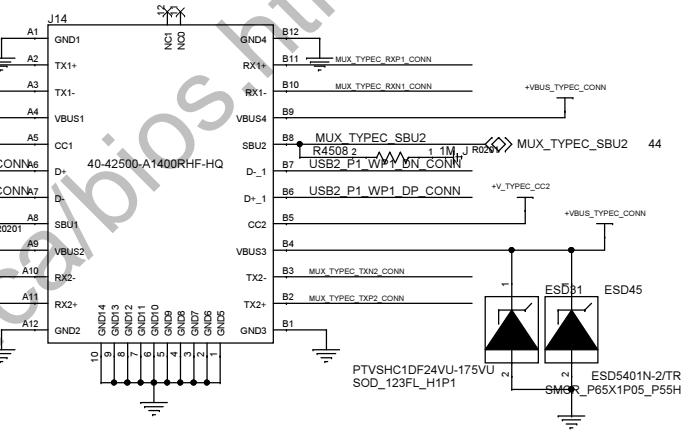
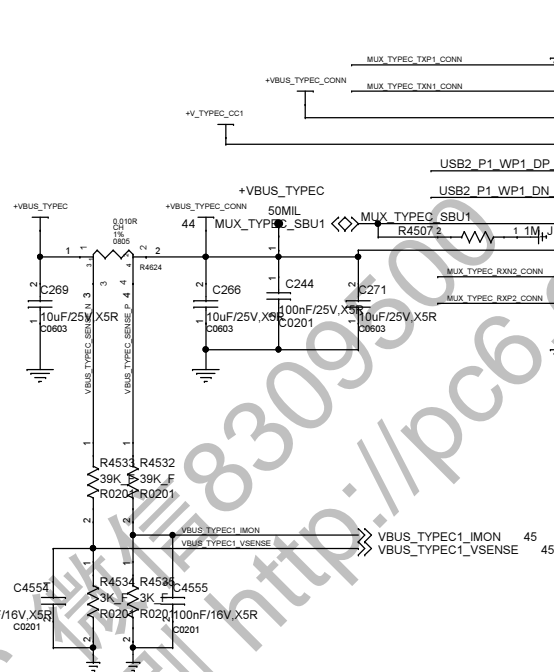
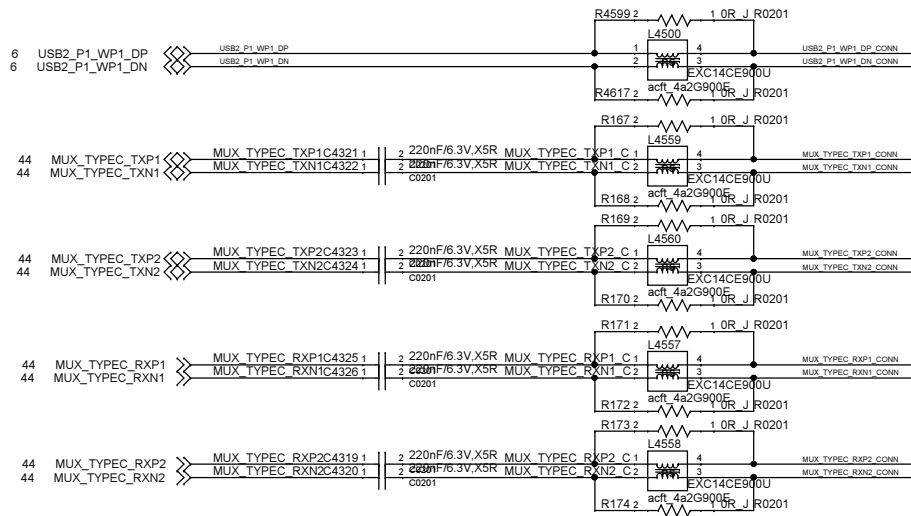




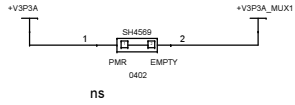




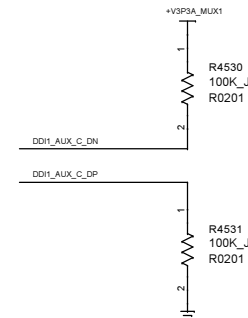
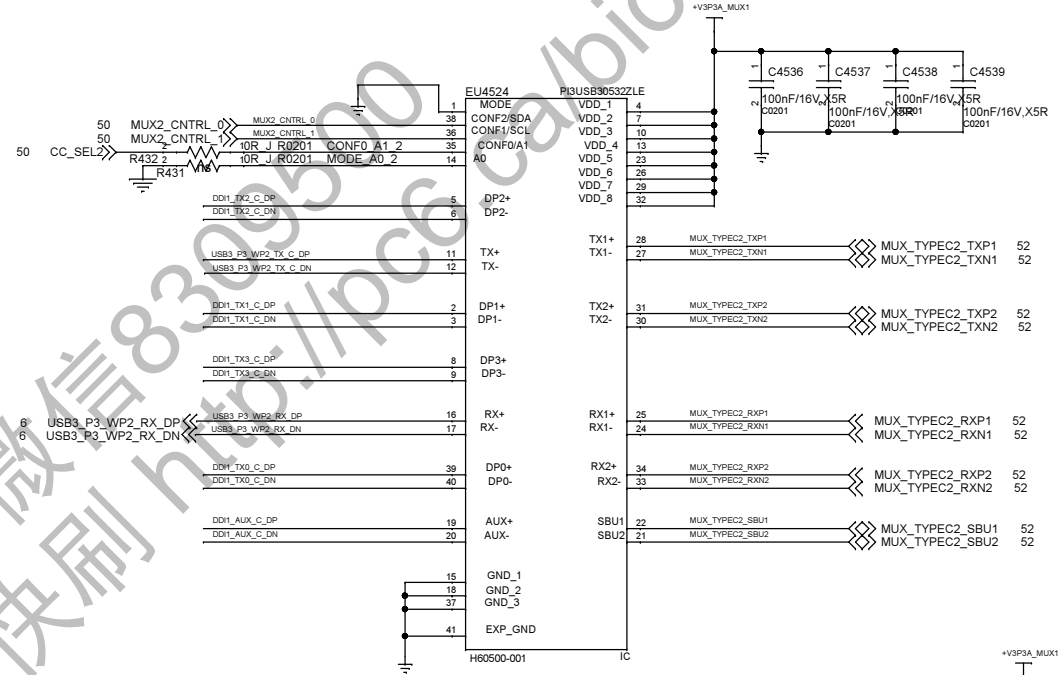
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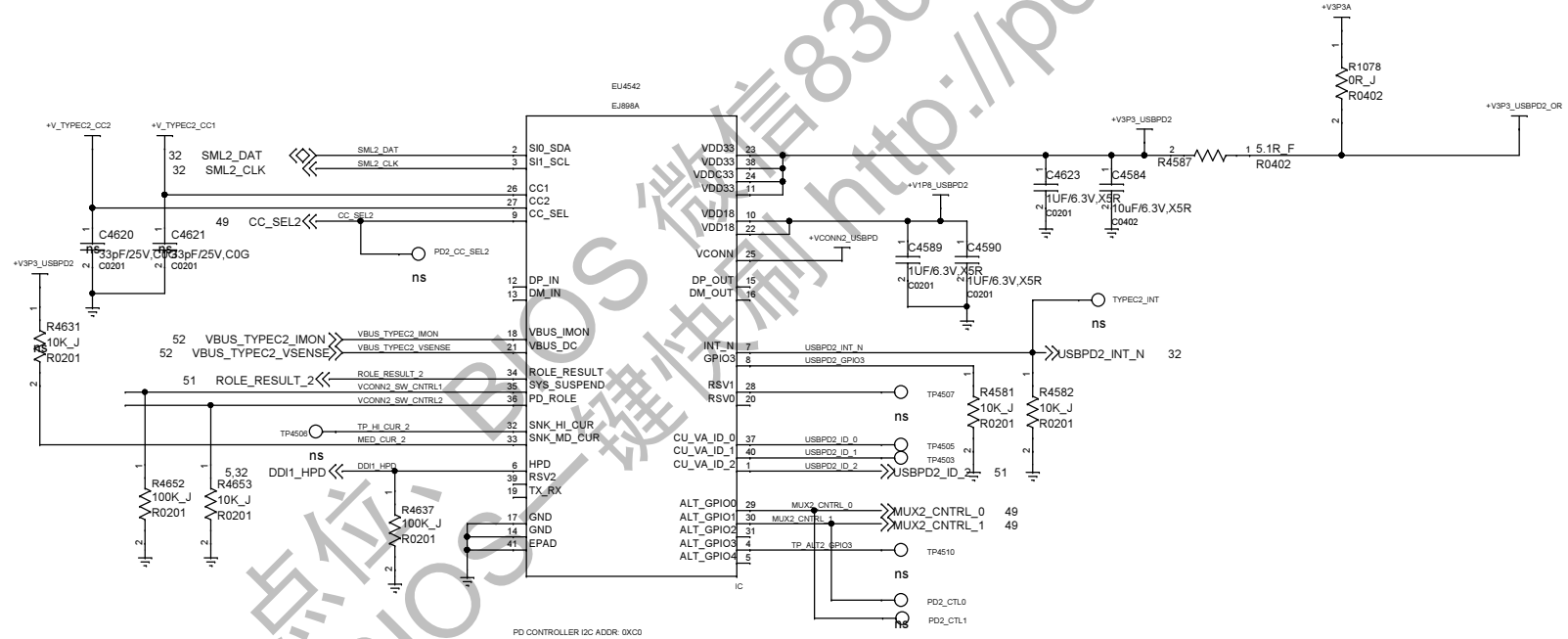
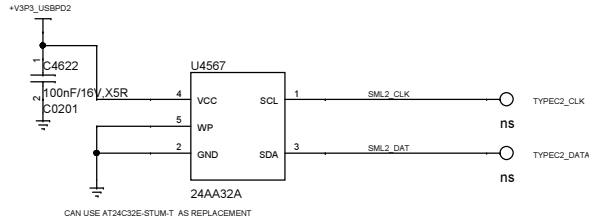


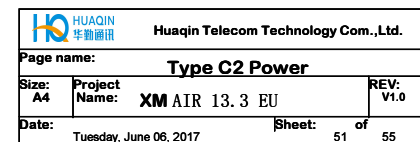


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5	DDI1_TX2_DP	>>	DDI1_TX2_DP	C4529	1	2	100nF/16V_X5R	DDI1_TX2_C_DP
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6	USB3_P3_WP2_TX_DN	>>	USB3_P3_WP2_TX_DN	C4532	1	2	100nF/16V_X5R	USB3_P3_WP2_TX_C_DN
6	USB3_P3_WP2_TX_DP	>>	USB3_P3_WP2_TX_DP	C4533	1	2	100nF/16V_X5R	USB3_P3_WP2_TX_C_DP
5	DDI1_AUX_DN	<<	DDI1_AUX_DN	C4534	1	2	100nF/16V_X5R	DDI1_AUX_C_DN
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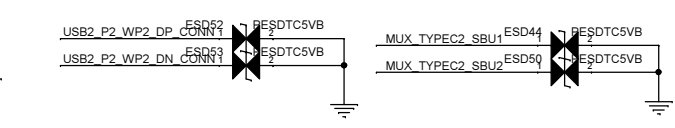
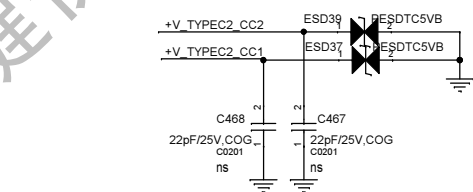
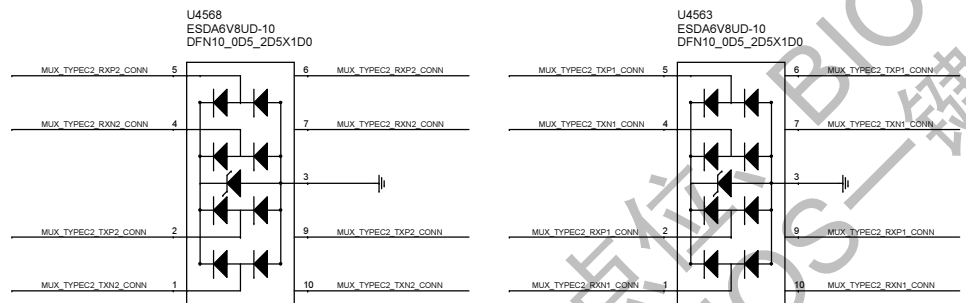
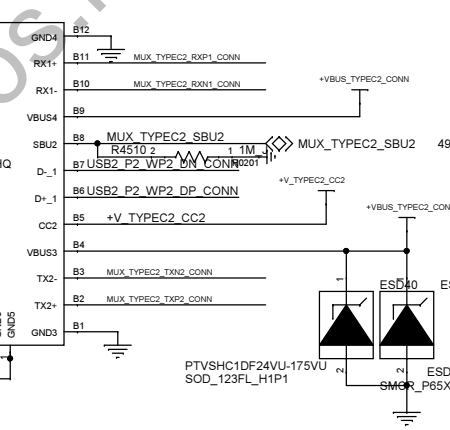
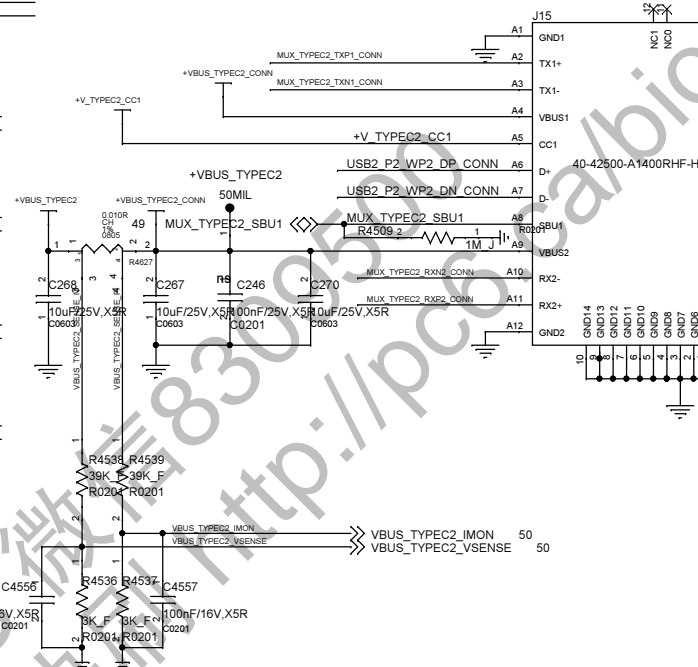
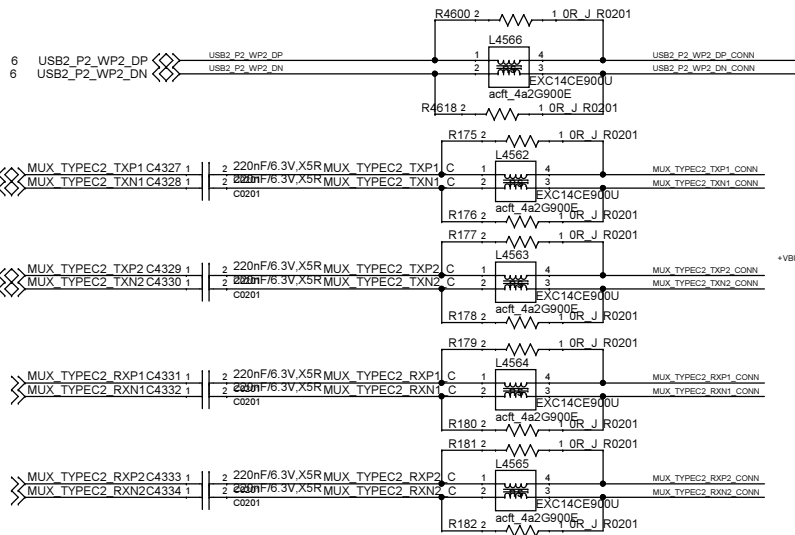


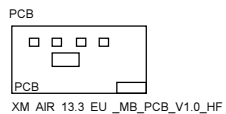
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 +V\_TYPEC2\_CC2 52



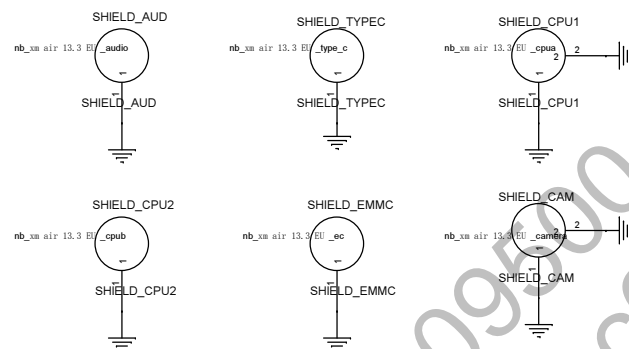


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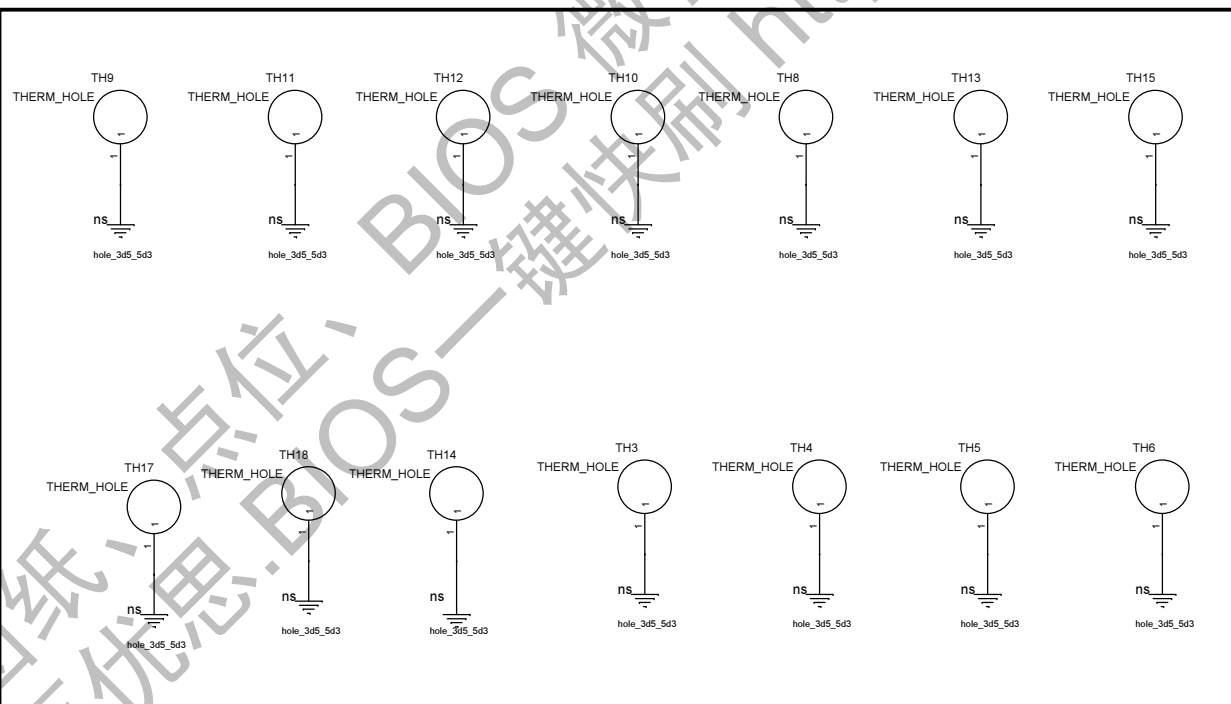




## SHIELD



## HOLE



## Changelist

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